Description

The VSM10N05 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

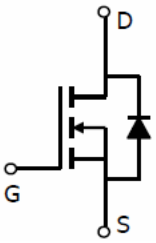
General Features

- V_{DS} = 60V,I_D =12A
  $R_{DS(ON)}$ < 7.6mΩ @ V_{GS}=10V (Typ:5.7mΩ)
  $R_{DS(ON)}$ < 8.0mΩ @ V_{GS}=4.5V (Typ:6.3mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Low gate to drain charge to reduce switching losses

Application

- Power switching application
- Load switch

SOP-8



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM10N05-S8	VSM10N05	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	50	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	15	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	10.6	A
Pulsed Drain Current	I_{DM}	30	A
Maximum Power Dissipation	P_D	3	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	42	℃/W

Electrical Characteristics (TC=25℃unless otherwise noted)

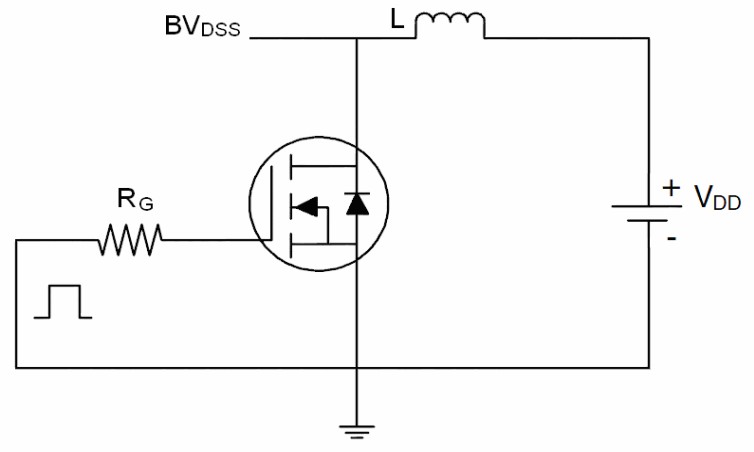
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	50		-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	0.9	1.2	1.8	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=12A	-	5.7	7.6	mΩ
		V_{GS}=4.5V, I_D=6A	-	6.3	8.0	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=12A	40	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=30V,V_{GS}=0V, F=1.0MHz	-	4100	-	PF
Output Capacitance	C_{oss}		-	298	-	PF
Reverse Transfer Capacitance	C_{rss}		-	229	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V, R_L=1Ω V_{GS}=10V,R_{GEN}=3Ω	-	8.5	-	nS
Turn-on Rise Time	t_r		-	7	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	40	-	nS
Turn-Off Fall Time	t_f		-	15	-	nS
Total Gate Charge	Q_g	V_{DS}=30V,I_D=12A, V_{GS}=10V	-	93	-	nC
Gate-Source Charge	Q_{gs}		-	9.7	-	nC
Gate-Drain Charge	Q_{gd}		-	20	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=15A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	15	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF=15A di/dt = 100A/μs (Note3)	-	32	-	nS
Reverse Recovery Charge	Qrr		-	45	-	nC

Notes:

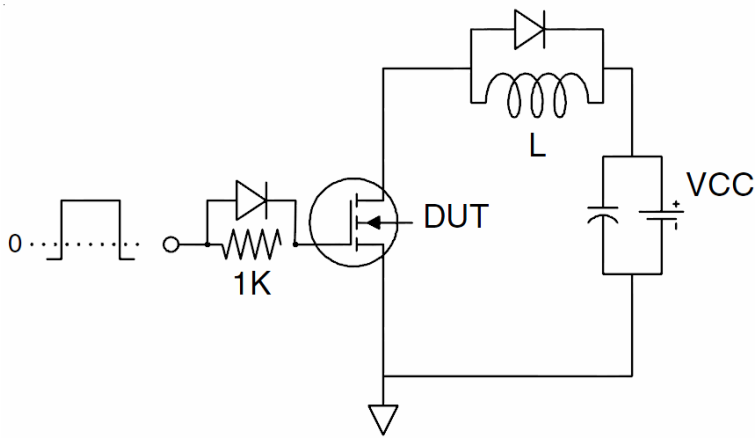
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Test Circuit

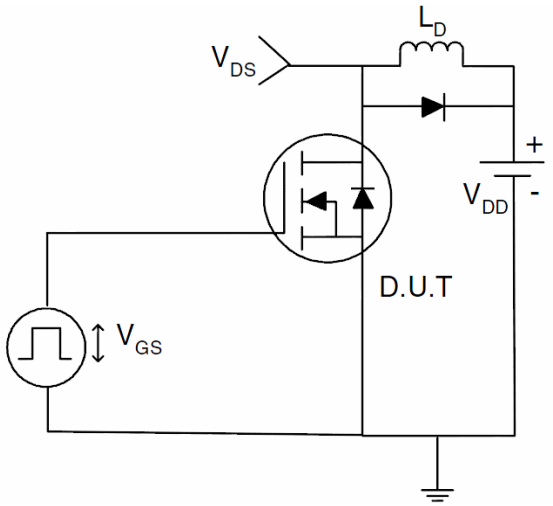
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

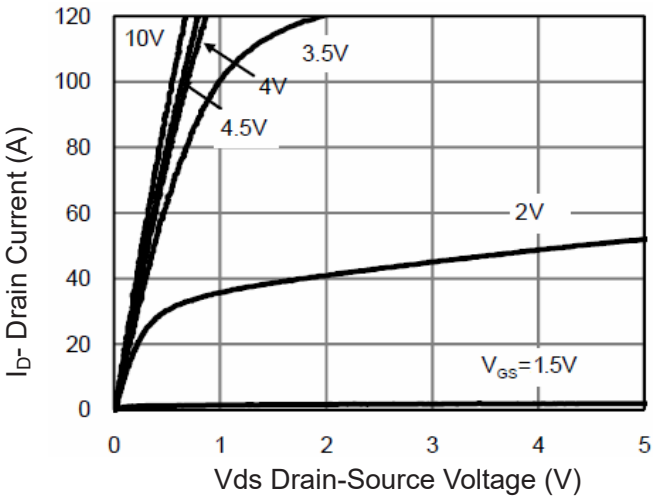


Figure 1 Output Characteristics

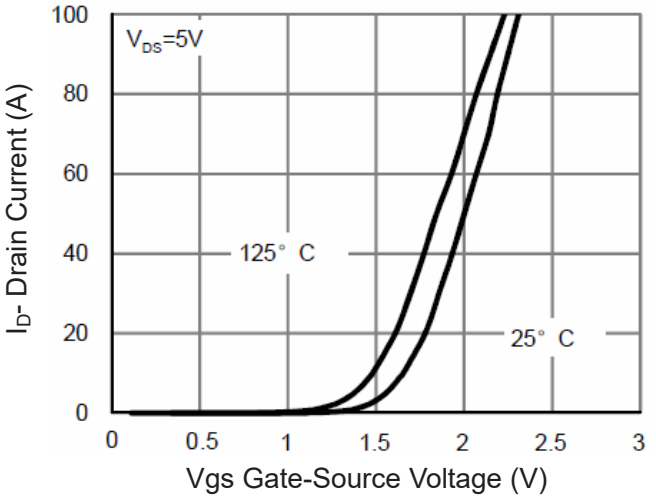


Figure 2 Transfer Characteristics

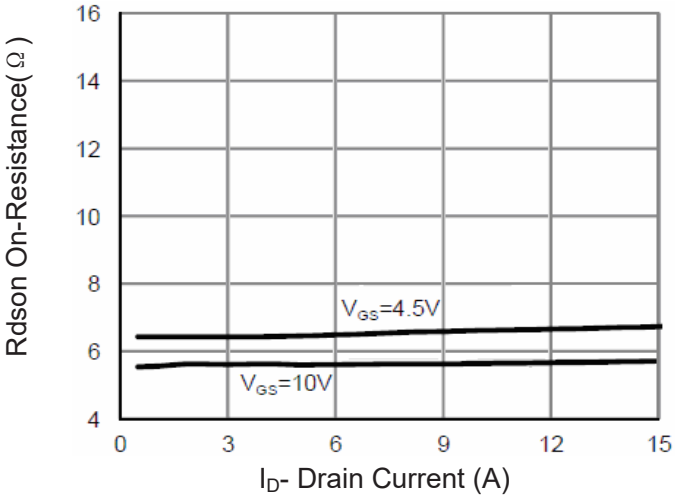


Figure 3 Rdson- Drain Current

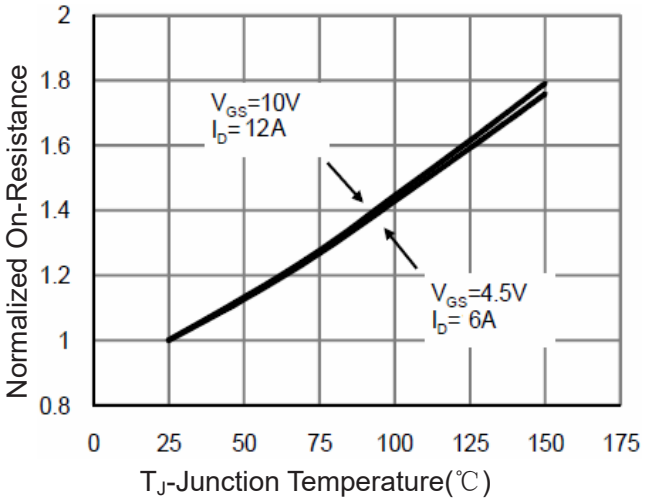


Figure 4 Rdson-JunctionTemperature

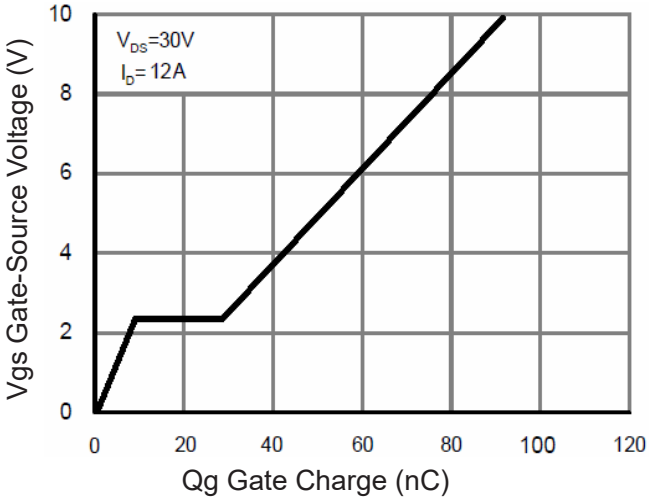


Figure 5 Gate Charge

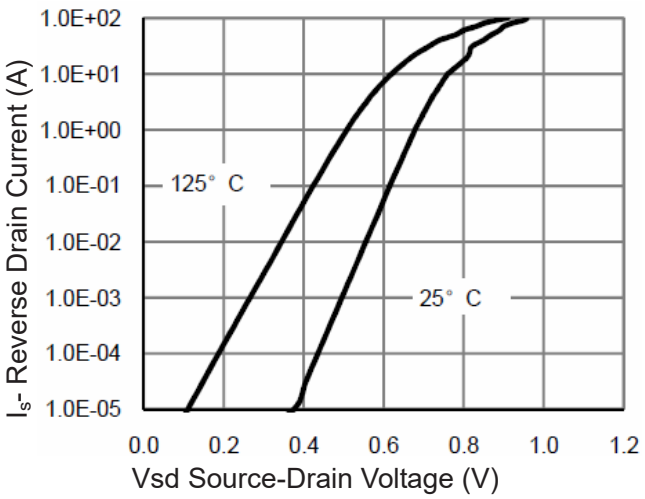


Figure 6 Source- Drain Diode Forward

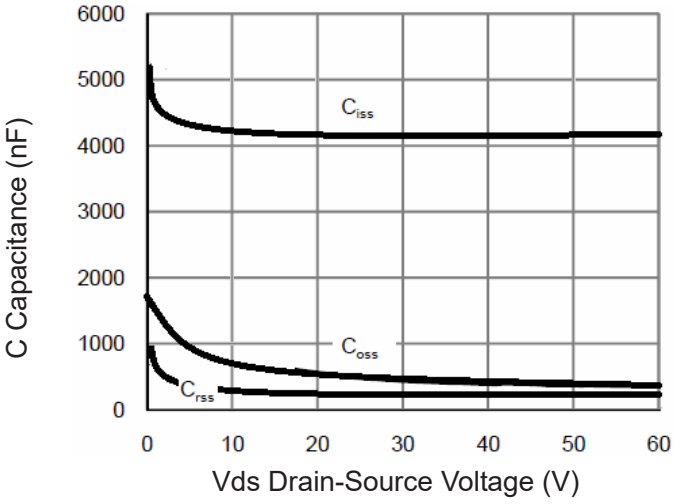


Figure 7 Capacitance vs Vds

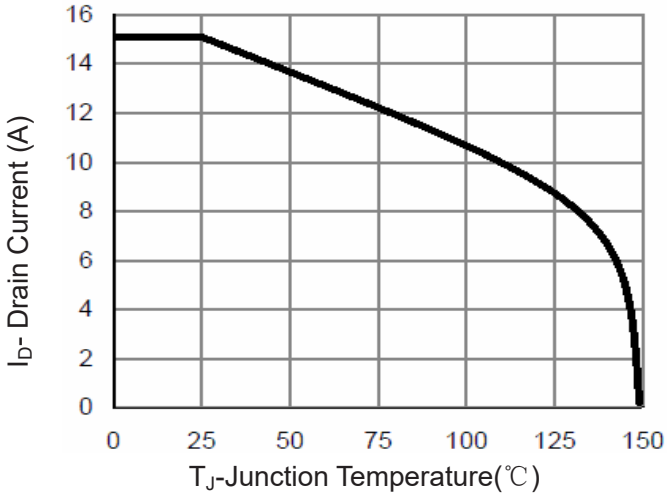


Figure 9 Current De-rating

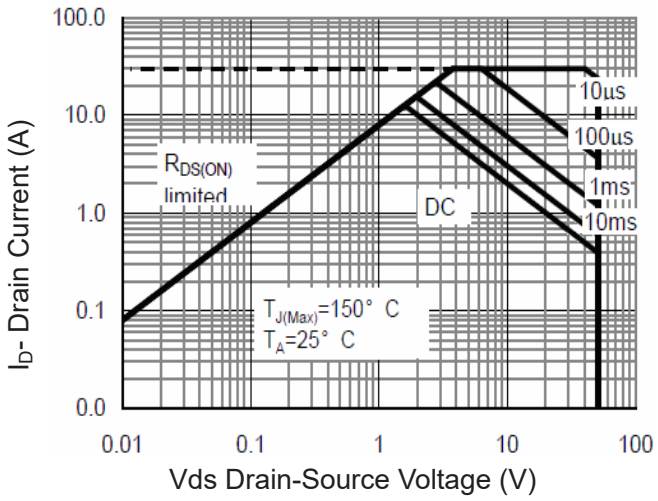


Figure 8 Safe Operation Area

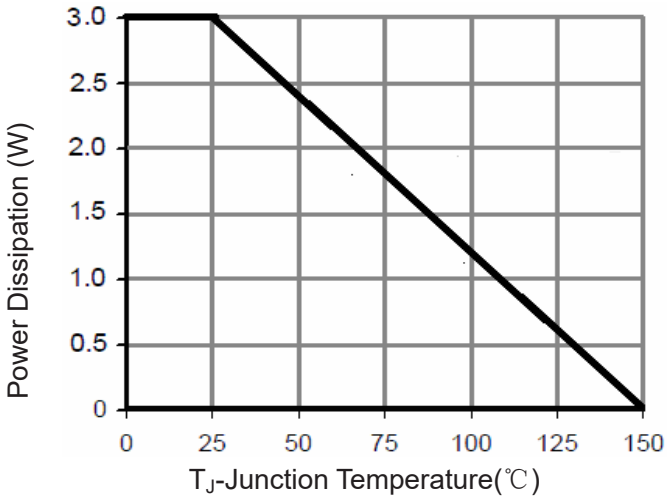


Figure 10 Power De-rating

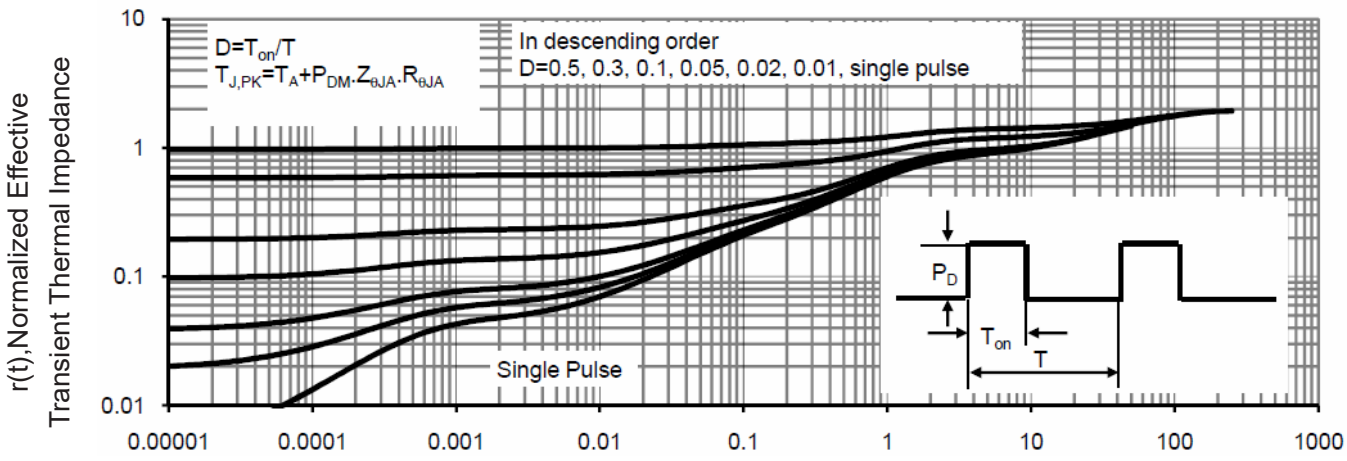


Figure 11 Normalized Maximum Transient Thermal Impedance