Description

The VSM150N06 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

● V_{DS} =60V, I_D =150A

   $R_{DS(ON)}$ <4.5mΩ @ V_{GS}=10V

● High density cell design for ultra low Rdson
● Fully characterized avalanche voltage and current
● Good stability and uniformity with high E_{AS}
● Excellent package for good heat dissipation
● Special process technology for high ESD capability

Application

● Power switching application
● Hard switched and high frequency circuits
● Uninterruptible power supply

TO-263
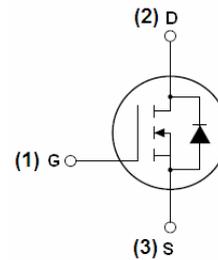
Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM150N06-T3	VSM150N06	TO-263	-	-	-

Absolute Maximum Ratings (T$_C$=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	150	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	105	A
Pulsed Drain Current	I_{DM}	600	A
Maximum Power Dissipation	P_D	220	W
Derating factor		1.47	W/℃
Single pulse avalanche energy [Note 5]	E_{AS}	1400	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	0.68	℃/W

Electrical Characteristics (T_C=25℃ unless otherwise noted)

| Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60	68	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics [Note 3]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=75A	-	3.6	4.5	mΩ
Forward Transconductance	g_{FS}	V_{DS}=50V,I_D=75A	180	-	-	S
Dynamic Characteristics [Note4]						
Input Capacitance	C_{Iss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	4644	-	PF
Output Capacitance	C_{oss}		-	460	-	PF
Reverse Transfer Capacitance	C_{rss}		-	426	-	PF
Switching Characteristics [Note 4]						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V,I_D=2A,R_L=15Ω V_{GS}=10V,R_G=2.5Ω	-	26	-	nS
Turn-on Rise Time	t_r		-	24	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	91	-	nS
Turn-Off Fall Time	t_f		-	39	-	nS
Total Gate Charge	Q_g	V_{DS}=30V,I_D=30A, V_{GS}=10V	-	113		nC
Gate-Source Charge	Q_{gs}		-	20		nC
Gate-Drain Charge	Q_{gd}		-	45		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage [Note 3]	V_{SD}	V_{GS}=0V,I_S=40A	-		1.2	V
Diode Forward Current [Note 2]	I_S		-	-	150	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 40A di/dt = 100A/μs[Note3]	-	42	60	nS
Reverse Recovery Charge	Qrr		-	66	80	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. Surface Mounted on FR4 Board, t ≤ 10 sec.

3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

5. EAS condition：Tj=25℃,V_{DD}=30V,V_G=10V,L=0.5mH,Rg=25Ω

Test circuit

### 1）E_{AS} test Circuits
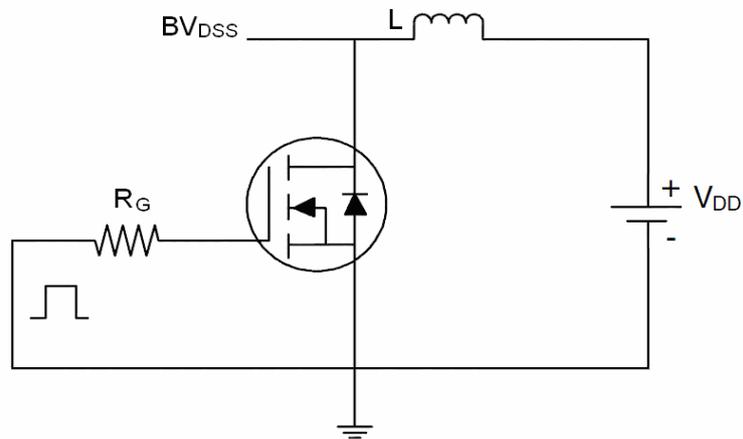
2）Gate charge test Circuit:
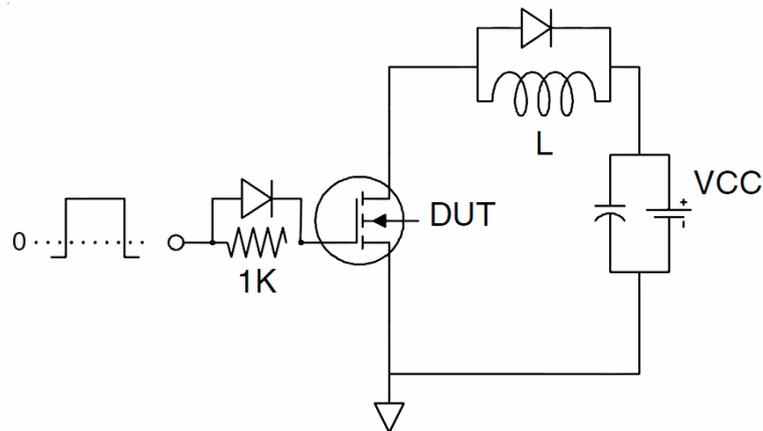
3）Switch Time Test Circuit:
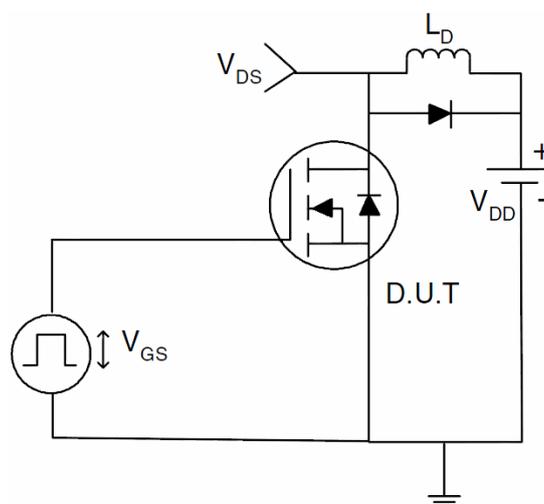
Typical Electrical and Thermal Characteristics (Curves)
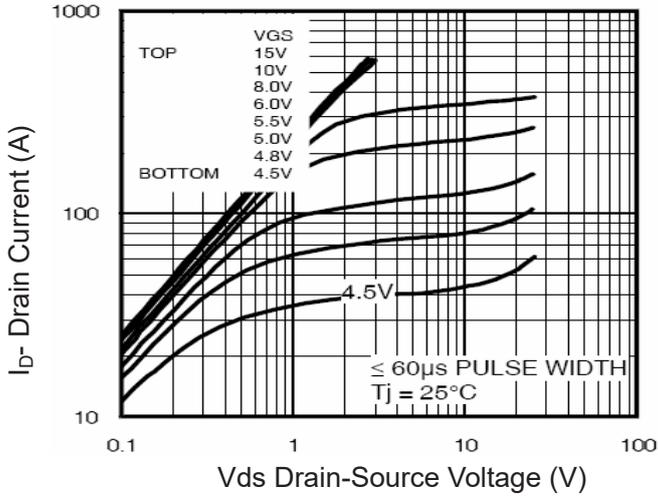
Figure 1 Output Characteristics
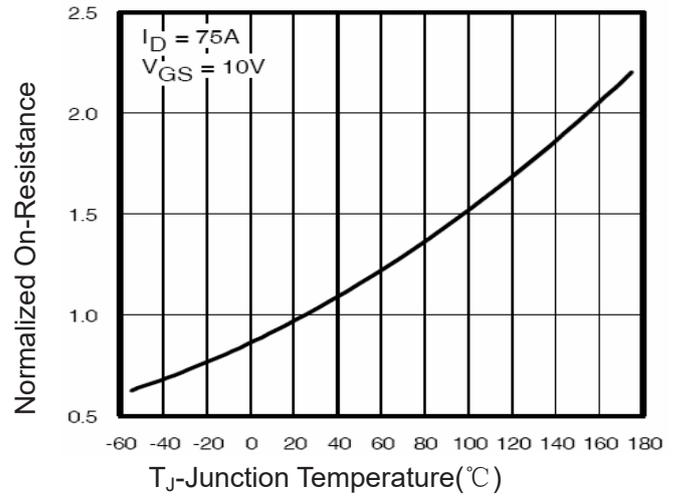
Figure 4 Rdson-JunctionTemperature
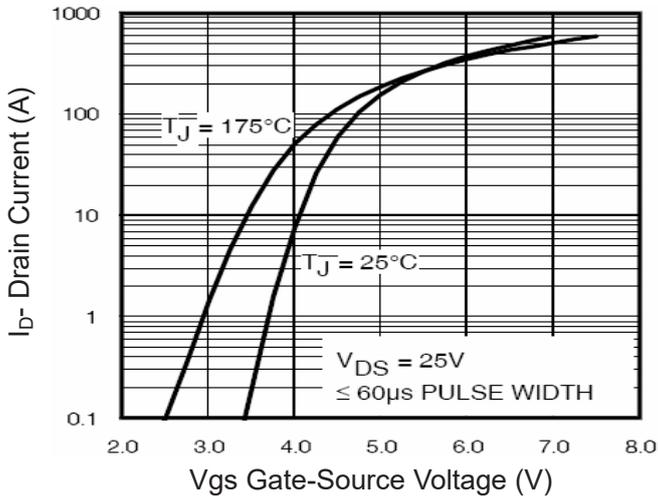
Figure 2 Transfer Characteristics
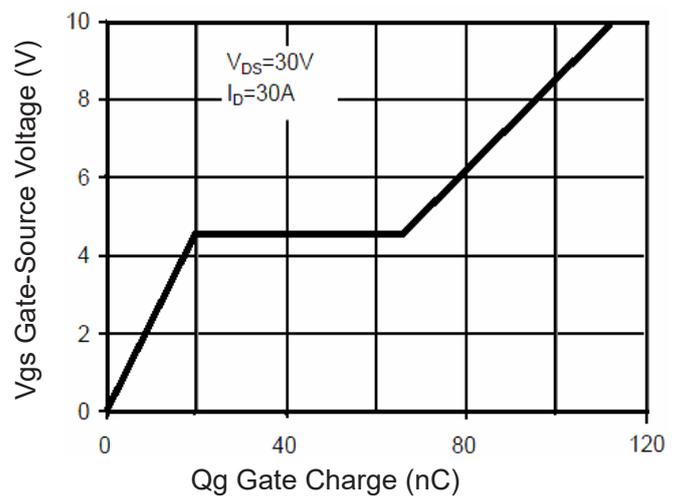
Figure 5 Gate Charge
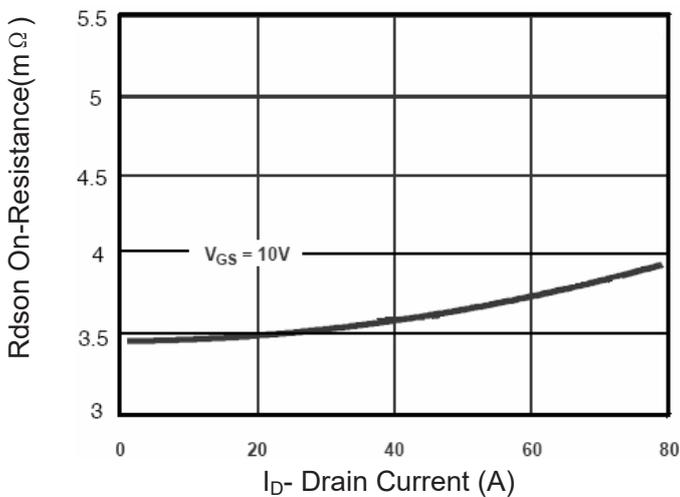
Figure 3 Rdson- Drain Current
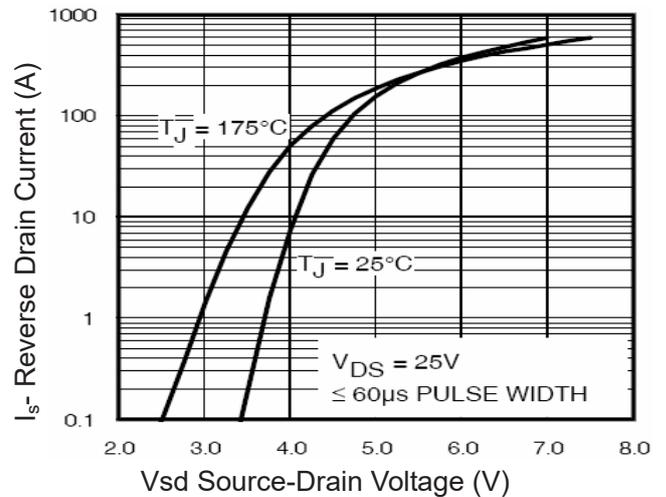
Figure 6 Source- Drain Diode Forward
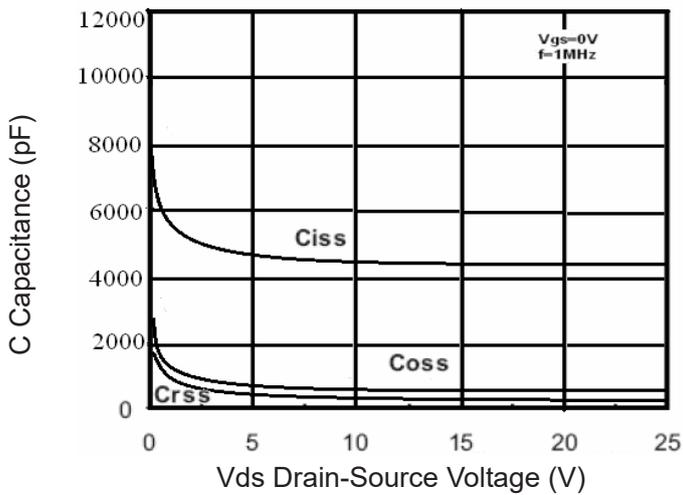
Figure 7 Capacitance vs Vds
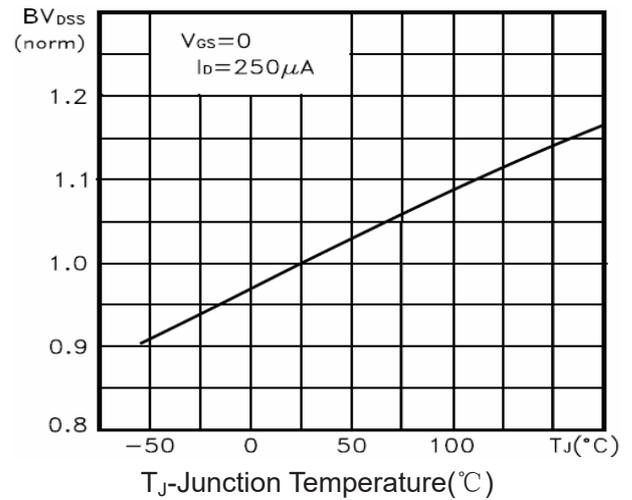
Figure 9   BV$_{DSS}$ vs Junction Temperature
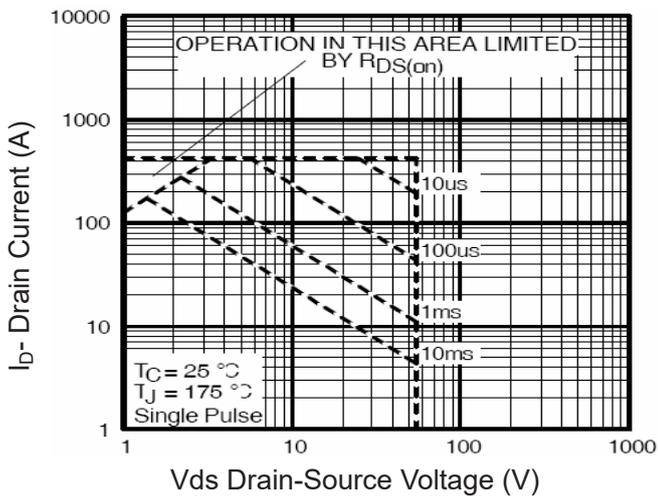
Figure 8   Safe Operation Area
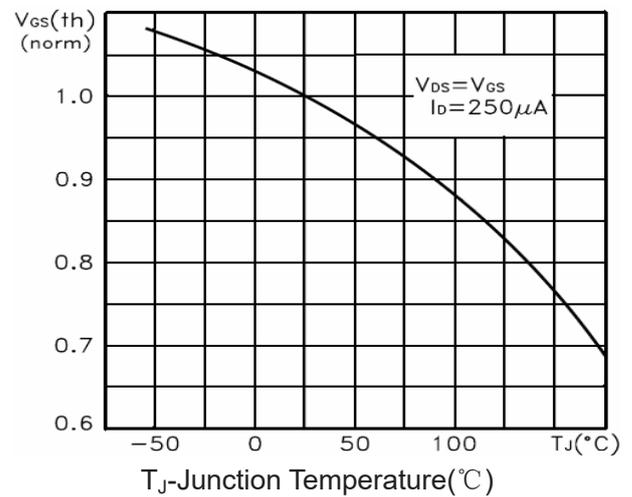
Figure 10   V$_{GS(th)}$ vs Junction Temperature

Square Wave Pluse Duration(sec)
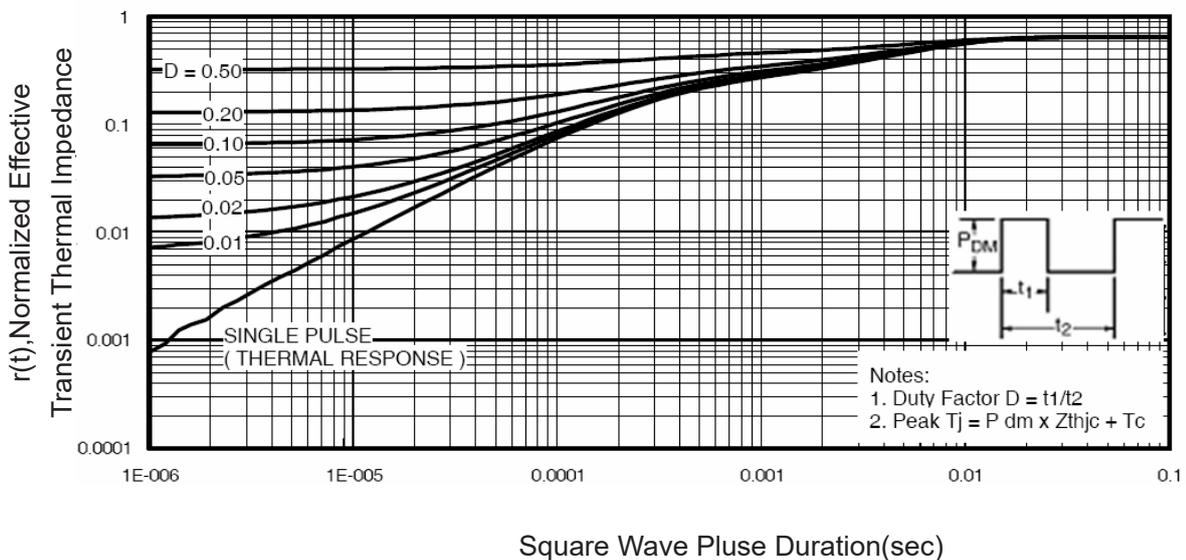
Figure 11 Normalized Maximum Transient Thermal Impedance