Description

The Power MOSFET is fabricated using the advanced planer **VDMOS** technology. The resulting device has low conduction resistance,superior switching performance and high avalanche energy.

Features

- Low $R_{DS(on)}$
- Low gate charge (typ. Q_g =50.7 nC)
- 100% UIS tested
- RoHS compliant

Applications

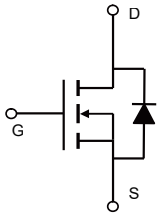
- Power factor correction.
- Switched mode power supplies.
- LED driver.

Product Summary

V_{DSS}	500V
I_D	17A
$R_{DS(on),max}$	0.33Ω
$Q_{g,typ}$	50.7 nC

Pin Configuration

TO-220F



Schematic

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	500	V
Continuous drain current (T_C = 25°C)	I_D	17	A
(T_C = 100°C)		9	A
Pulsed drain current [1]	I_{DM}	68	A
Gate-Source voltage	V_{GSS}	±30	V
Avalanche energy, single pulse [2]	E_{AS}	1037	mJ
Power Dissipation (T_C = 25°C)	P_D	36.7	W
Operating junction and storage temperature range	T_J, T_{STG}	-55 to +150	°C
Continuous diode forward current	I_S	17	A
Diode pulse current	$I_{S,pulse}$	68	A

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, Junction-to-case	$R_{\theta JC}$	3.4	°C/W
Thermal resistance, Junction-to-ambient[3]	$R_{\theta JA}$	65	°C/W

Package Marking and Ordering Information

Device	Device Package	Marking	Units/Tube
VSM17N50-TF	TO-220F	VSM17N50-TF	50

Electrical Characteristics

T_c = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0 V, I_D=0.25 mA	500	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.25 mA	2	-	4	V
Drain cut-off current	I_{DSS}	V_{DS}=500 V, V_{GS}=0 V, T_j = 25°C T_j = 150°C	 - -	 -	 1 100	μA
Gate leakage current, Forward	I_{GSSF}	V_{GS}=30 V, V_{DS}=0 V	-	-	100	nA
Gate leakage current, Reverse	I_{GSSR}	V_{GS}=-30 V, V_{DS}=0 V	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=8.5A,T_J=25℃	-	0.26	0.33	Ω
Gate resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz	-	1.2	-	Ω
Dynamic characteristics						
Input capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V,	-	2655	-	pF
Output capacitance	C_{oss}	f = 1 MHz	-	251	-	
Reverse transfer capacitance	C_{rss}		-	1.9	-	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 17A	-	14.5	-	ns
Rise time	t_r	R_G = 10 Ω, V_{GS}=15 V	-	39.6	-	
Turn-off delay time	$t_{d(off)}$		-	89	-	
Fall time	t_f		-	11	-	
Gate charge characteristics						
Gate to source charge	Q_{gs}	V_{DD}=400 V, I_D=17 A,	-	12.6	-	nC
Gate to drain charge	Q_{gd}	V_{GS}=0 to 10 V	-	18	-	
Gate charge total	Q_g		-	50.7	-	
Gate plateau voltage	$V_{plateau}$		-	5	-	V
Reverse diode characteristics						
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=17 A	-	-	1.5	V
Reverse recovery time	t_{rr}	V_R=400 V, I_F=17A,	-	366	-	ns
Reverse recovery charge	Q_{rr}	dI_F/dt=100 A/μs	-	4.2	-	μC
Peak reverse recovery current	I_{rrm}		-	23	-	A

Notes:

1. Pulse width limited by maximum junction temperature.

2. VDD=60V,L=10mH, I_{AS} = 14.4A, Starting T_j= 25°C.

3: The value of R_{thJA} is measured by placing the device in a still air box which is one cubic foot.

Electrical Characteristics Diagrams

Figure 1. Typical Output Characteristics

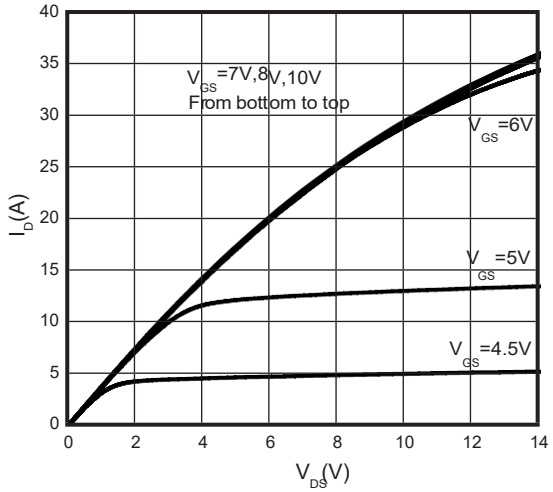


Figure 2. Transfer Characteristics

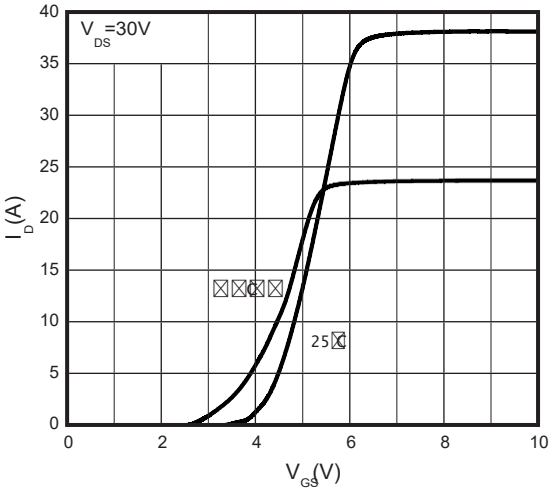


Figure 3. On-Resistance vs. Drain Current

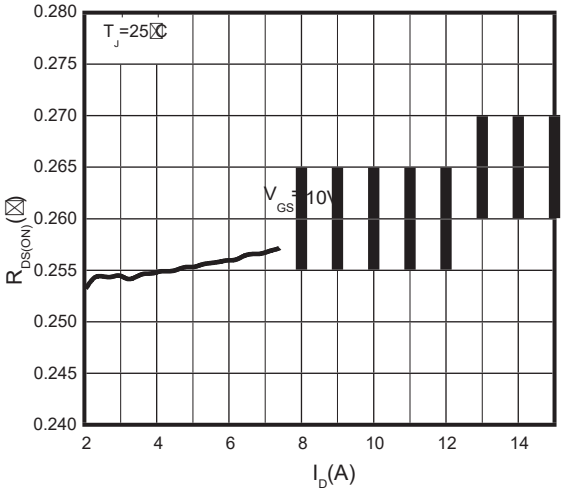


Figure 4. On-Resistance vs. Temperature

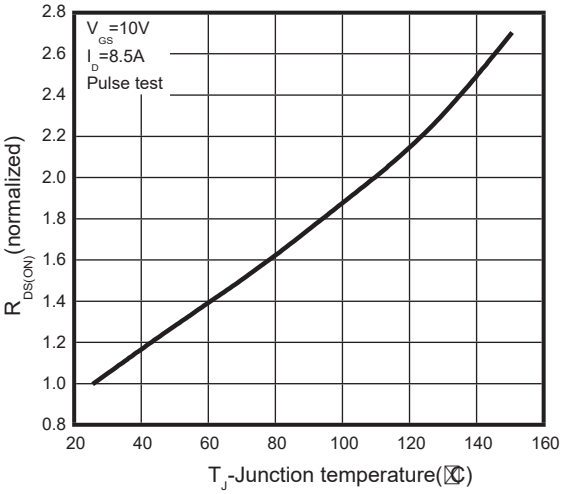


Figure 5. Breakdown Voltage vs. Temperature

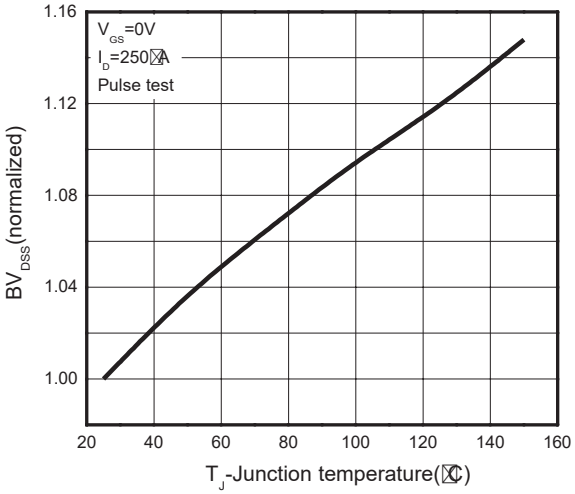


Figure 6.Threshold Voltage vs. Temperature

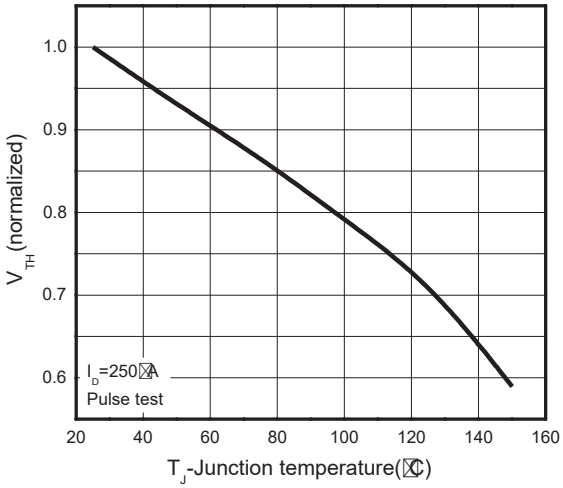


Figure 7.Rds(on) vs. Gate Voltage

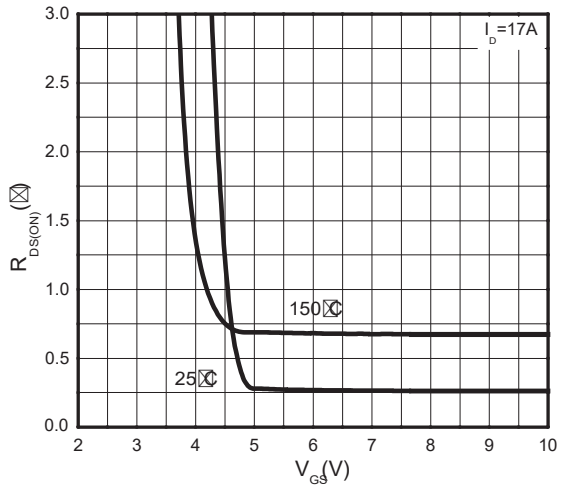


Figure 8.Body-Diode Characteristics

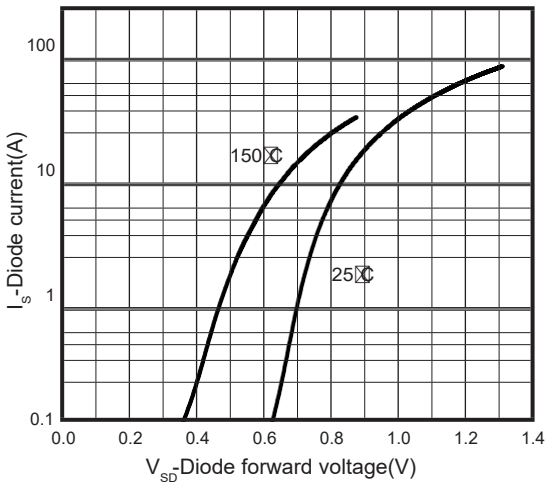


Figure 9. Capacitance Characteristics

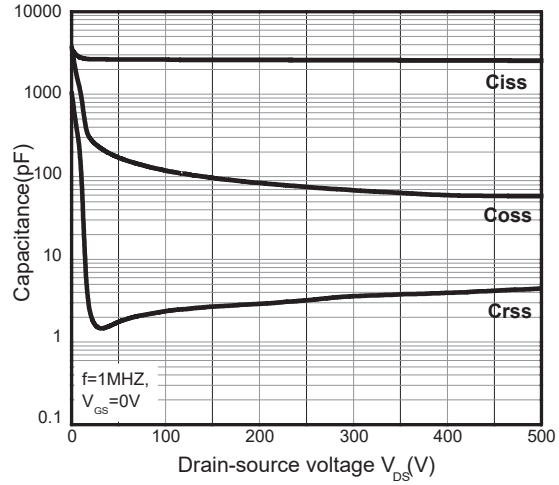


Figure 10. Gate Charge Characteristics

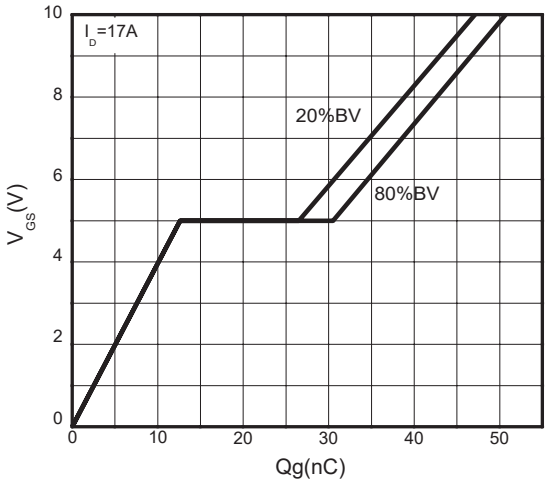


Figure 11. Continuous Drain Current vs. Temperature

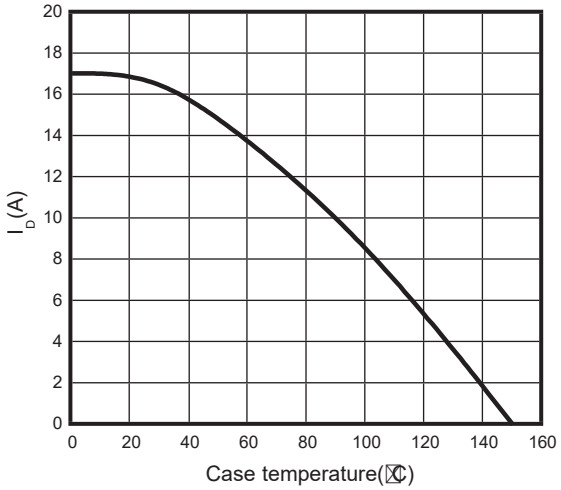


Figure 12. Power Dissipation vs. Temperature

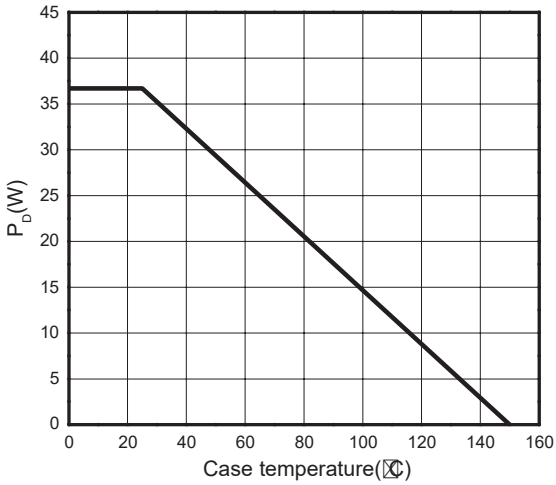


Figure 13: Safe Operating Area

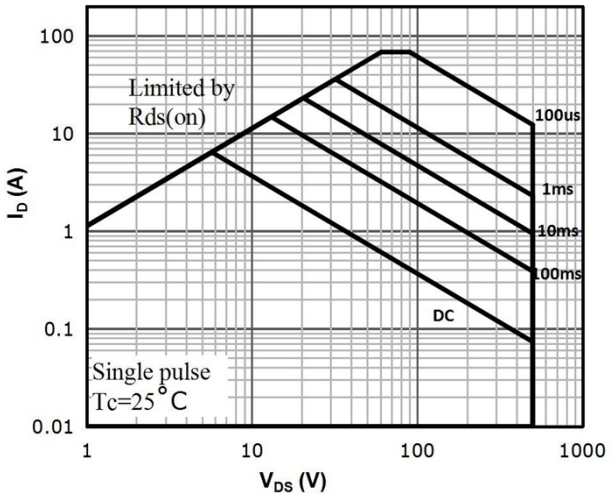
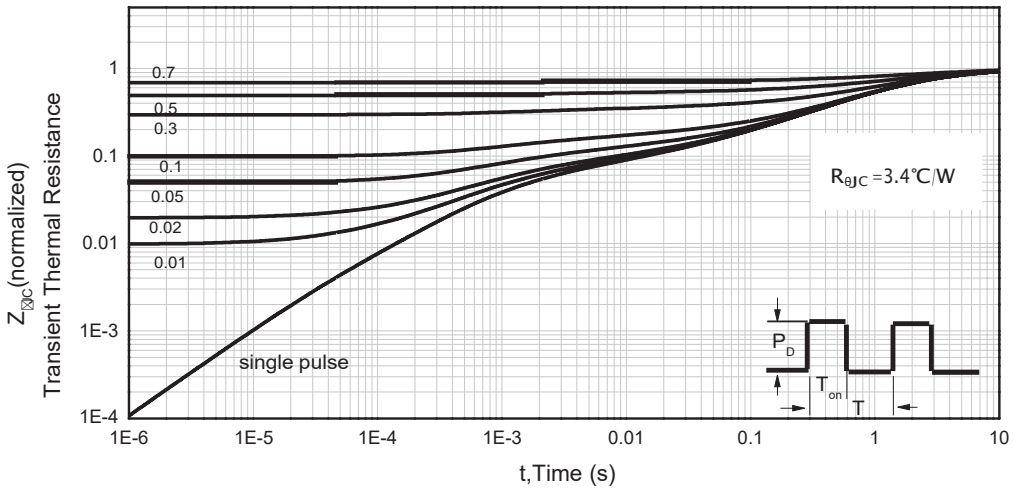
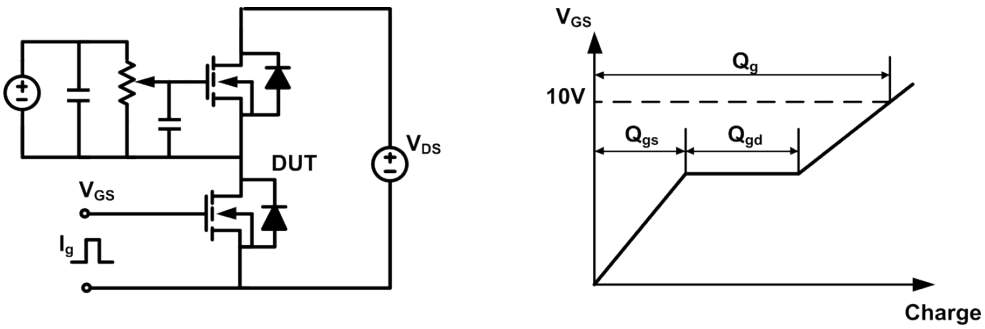


Figure 14. Transient Thermal Impedance, Junction to Case

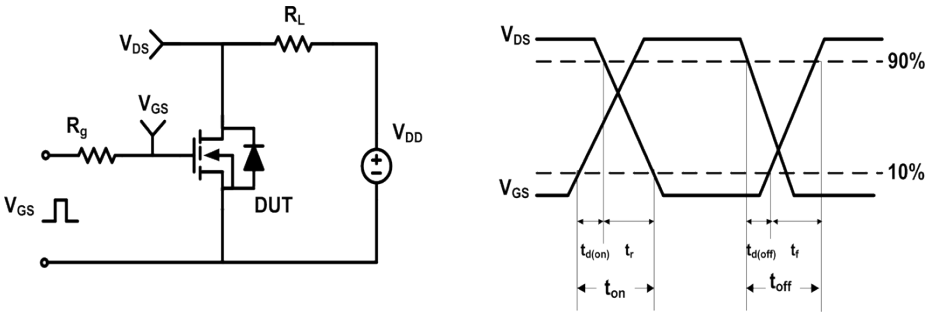


Test Circuit & Waveforms

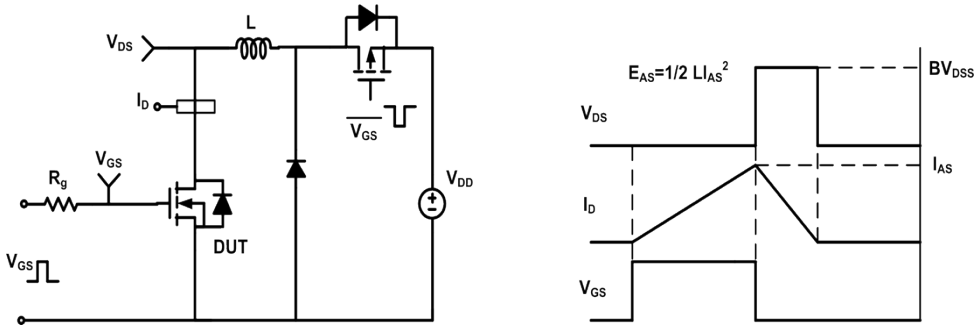
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveform



Diode Recovery Test Circuit & Waveform