

### Description

The VSM20P06 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is well suited for high current load applications.

### General Features

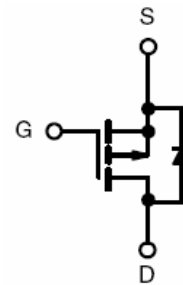
- $V_{DS} = -60V, I_D = -20A$   
 $R_{DS(ON)} < 70m\Omega @ V_{GS} = -10V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

### Application

- High side switch for full bridge converter
- DC/DC converter for LCD display



TO-220C



Schematic Diagram

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM20P06-TC	VSM20P06	TO-220C	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-20	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	-14	A
Pulsed Drain Current	$I_{DM}$	-30	A
Maximum Power Dissipation	$P_D$	60	W
Derating factor		0.48	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	264	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

**Thermal Characteristic**

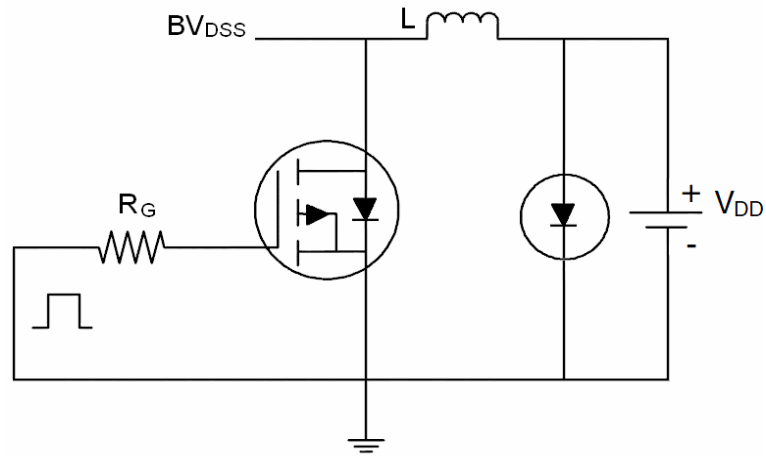
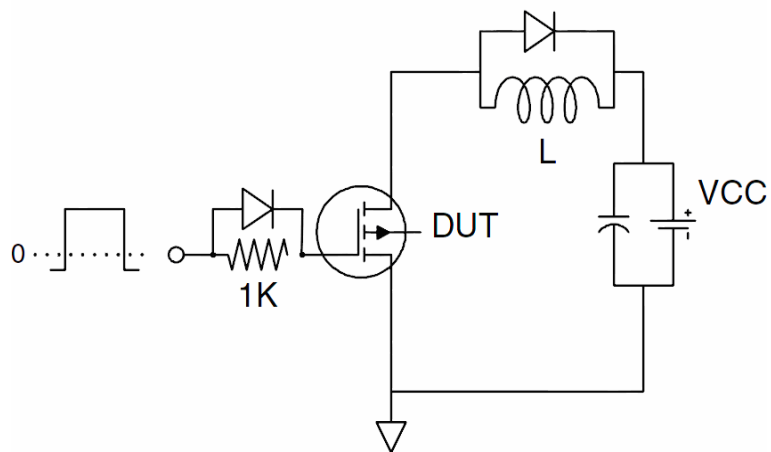
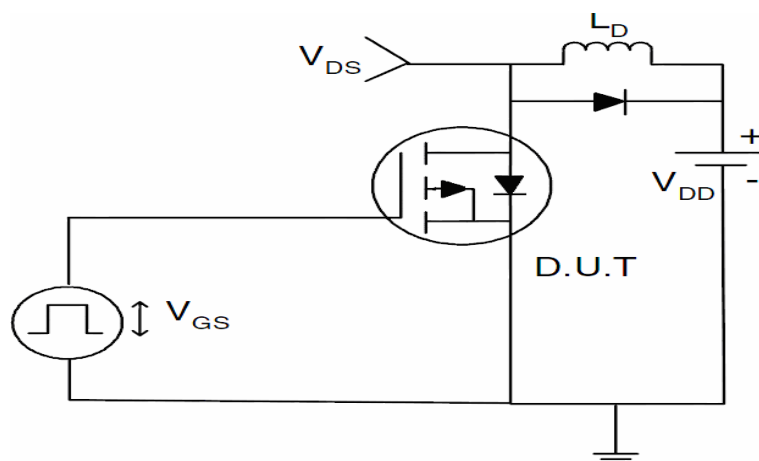
Thermal Resistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	2.1	$^{\circ}\text{C}/\text{W}$
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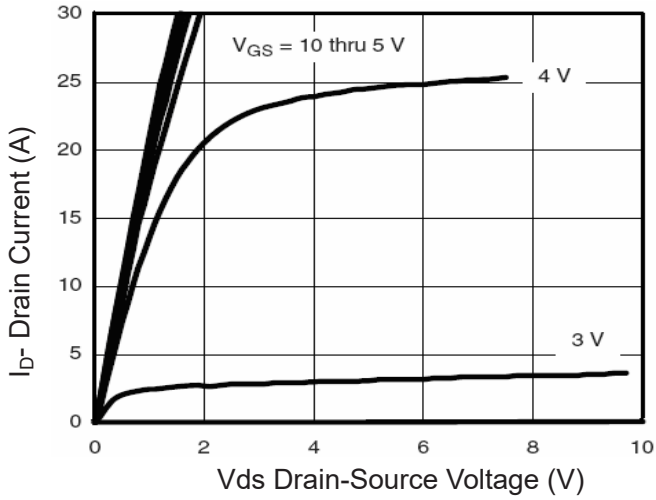
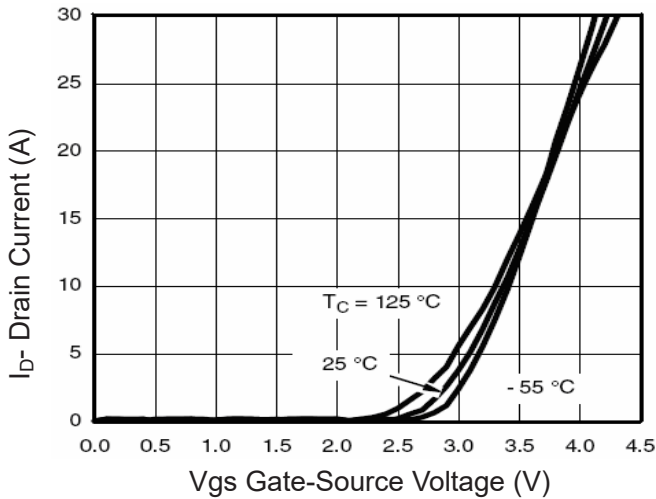
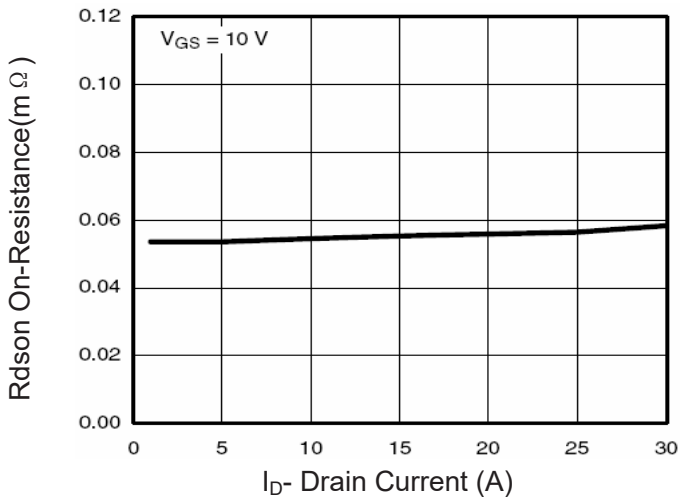
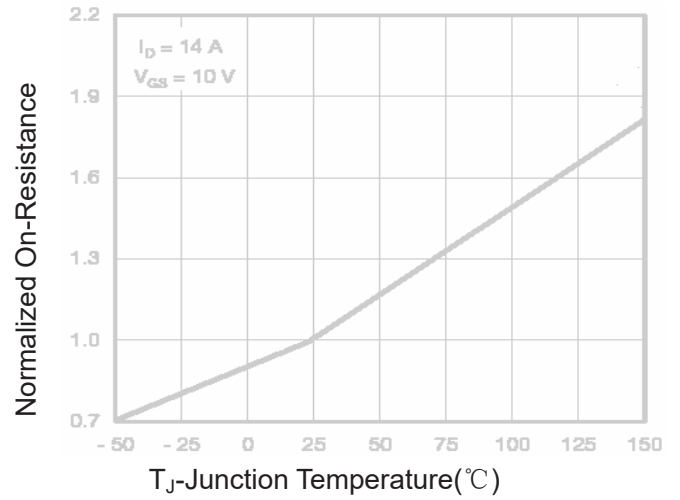
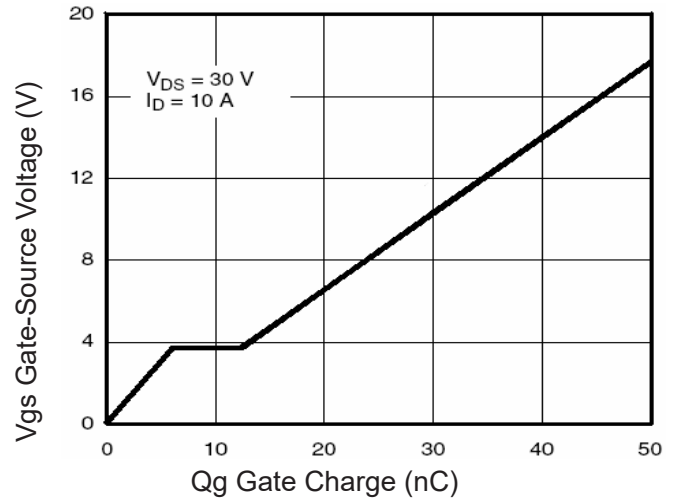
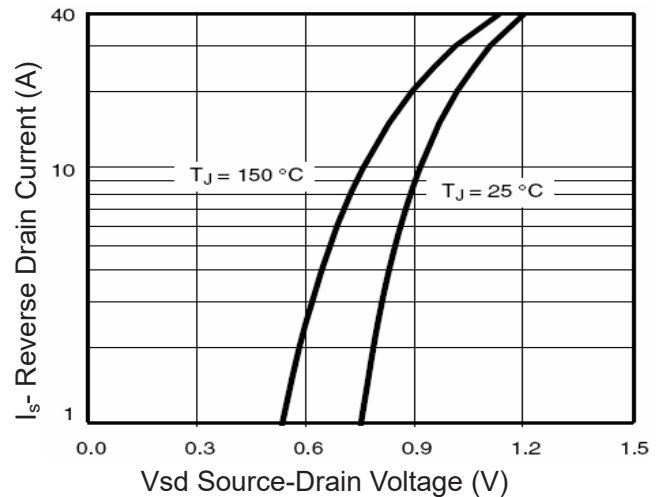
**Electrical Characteristics ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)**

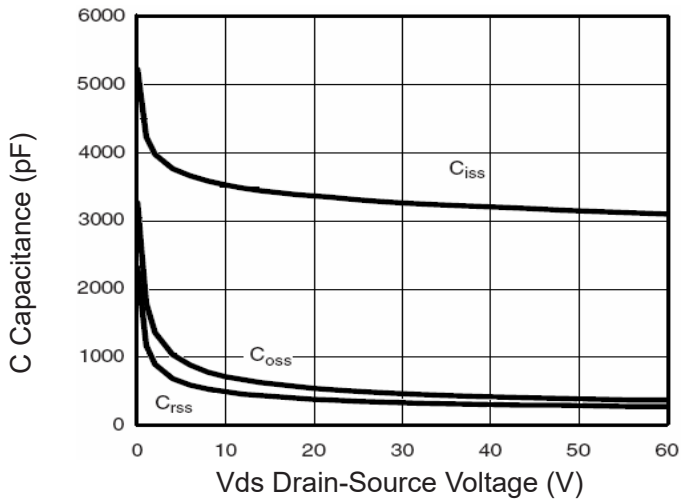
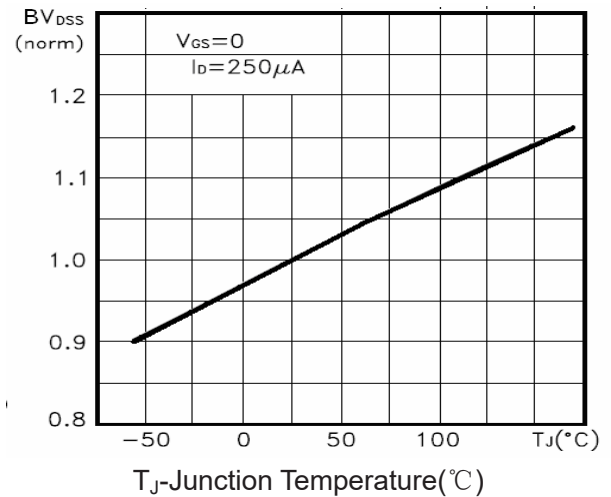
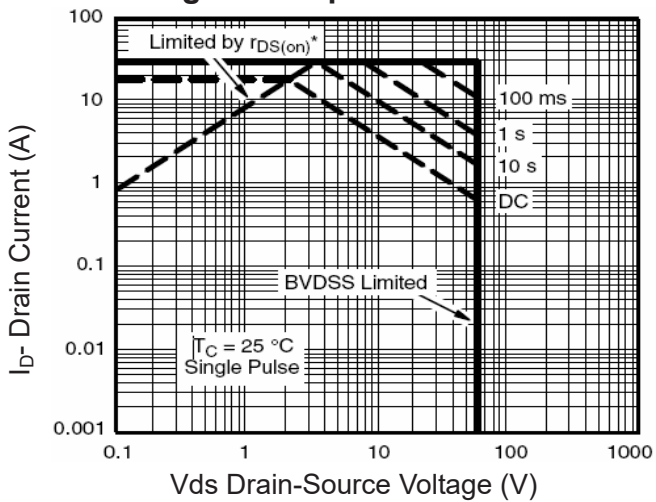
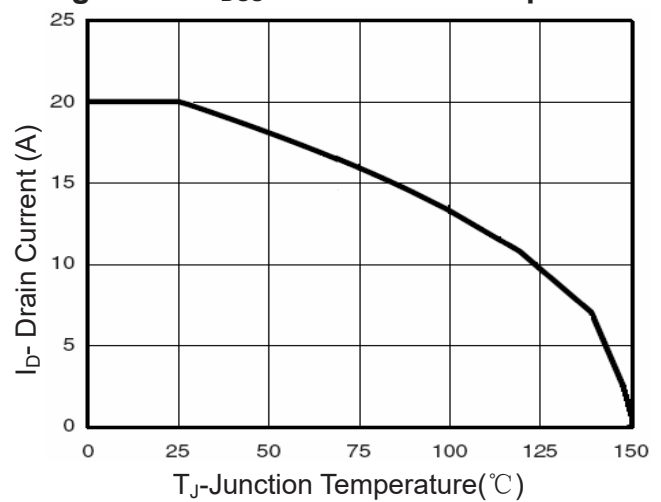
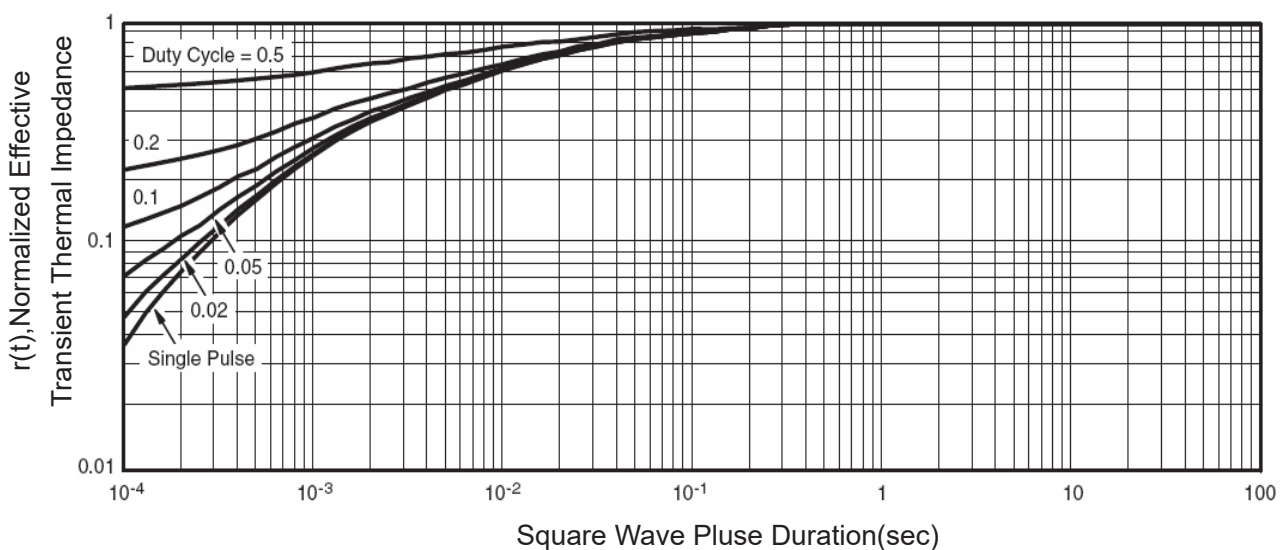
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-60	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-60V, V_{GS}=0V$	-	-	-1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.2	-1.9	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-10A$	-	54	70	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-10V, I_D=-10A$	-	20	-	S
<b>Dynamic Characteristics (Note4)</b>						
Input Capacitance	$C_{ISS}$	$V_{DS}=-25V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	3430	-	PF
Output Capacitance	$C_{OSS}$		-	391	-	PF
Reverse Transfer Capacitance	$C_{RSS}$		-	272	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-30V, R_L=3\Omega,$ $V_{GS}=-10V, R_G=2.5\Omega$	-	9	-	nS
Turn-on Rise Time	$t_r$		-	10	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	70	-	nS
Turn-Off Fall Time	$t_f$		-	35	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-30, I_D=-10A,$ $V_{GS}=-10V$	-	30	-	nC
Gate-Source Charge	$Q_{gs}$		-	5.5	-	nC
Gate-Drain Charge	$Q_{gd}$		-	6.5	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=-10A$	-	-	-1.2	V
Diode Forward Current (Note 2)	$I_S$		-	-	-20	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}, I_F = -10A$ $di/dt = -100A/\mu s(\text{Note3})$	-	43	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	41	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition:  $T_J=25^{\circ}\text{C}, V_{DD}=-20V, V_G=-10V, L=1\text{mH}, R_g=25\Omega, I_{AS}=23A$

**Test Circuit**
**1) E<sub>AS</sub> Test Circuit**

**2) Gate Charge Test Circuit**

**3) Switch Time Test Circuit**


**Typical Electrical and Thermal Characteristics (Curves)**

**Figure 1 Output Characteristics**

**Figure 2 Transfer Characteristics**

**Figure 3 Rdson- Drain Current**

**Figure 4 Rdson-Junction Temperature**

**Figure 5 Gate Charge**

**Figure 6 Source- Drain Diode Forward**


**Figure 7 Capacitance vs Vds**

**Figure 9  $BV_{DSS}$  vs Junction Temperature**

**Figure 8 Safe Operation Area**

**Figure 10  $I_D$  Current Derating vs Junction Temperature**

**Figure 11 Normalized Maximum Transient Thermal Impedance**