Description

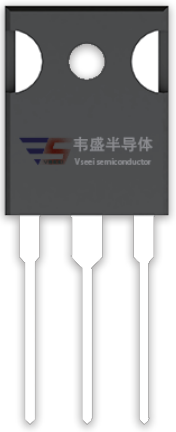
The VSM210N10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of other applications.

General Features

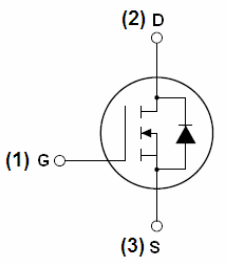
- V_{DSS} =100V,I_D =210A
  $R_{DS(ON)}$ < 4.2mΩ @ V_{GS}=10V （Typ：3.3 mΩ）
- Good stability and uniformity with high E_{AS}
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- DC motor drive
- High efficiency synchronous rectification in SMPS
- Uninterruptible power supply
- High speed power switching
- Hard switched and high frequency circuits



TO-247



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM210N10-T7	VSM210N10	TO-247	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	210	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	140	A
Pulsed Drain Current	I_{DM}	850	A
Maximum Power Dissipation	P_D	385	W
Derating factor		2.57	W/℃

Single pulse avalanche energy (Note 3)	E_{AS}	2300	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	13	V/ns
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 1)	$R_{\theta JC}$	0.39	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

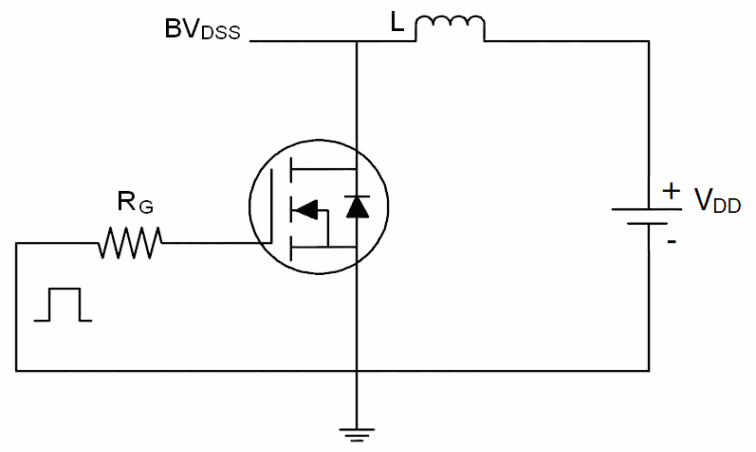
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	100	110	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±200	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.5	3.5	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=40A	-	3.3	4.2	mΩ
Forward Transconductance	g_{FS}	V_{DS}=25V,I_D=40A	300	-	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	13500	-	PF
Output Capacitance	C_{oss}		-	862	-	PF
Reverse Transfer Capacitance	C_{rss}		-	659	-	PF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V,I_D=2A V_{GS}=10V,R_{GEN}=2.5Ω (Note2)	-	68	-	nS
Turn-on Rise Time	t_r		-	45	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	215	-	nS
Turn-Off Fall Time	t_f		-	56	-	nS
Total Gate Charge	Q_g	V_{DS}=30V,I_D=30A, V_{GS}=10V(Note2)	-	304	-	nC
Gate-Source Charge	Q_{gs}		-	64	-	nC
Gate-Drain Charge	Q_{gd}		-	95	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=40A	-	-	1.2	V
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 75A di/dt = 100A/μs(Note2)	-	65	-	nS
Reverse Recovery Charge	Qrr		-	98	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

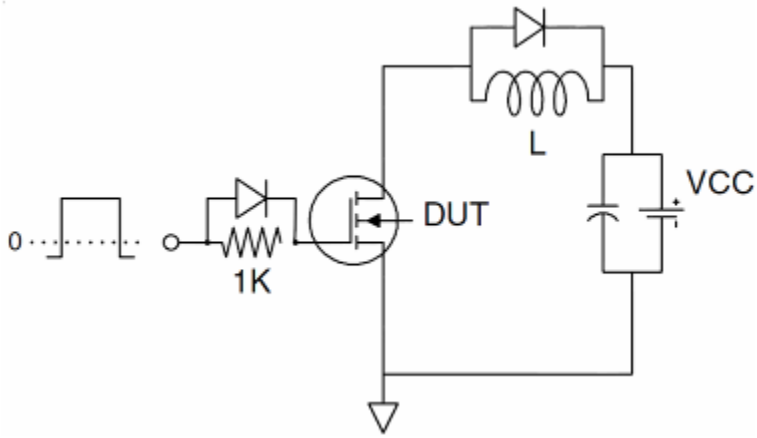
1. Surface Mounted on FR4 Board, t ≤ 10 sec.
2. Pulse Test: Pulse Width ≤ 400μs, Duty Cycle ≤ 2%.
3. EAS condition：Tj=25℃,V_{DD}=37.5V,V_G=10V,L=2mH,Rg=25Ω,I_{AS}=37A
4. I_{SD}≤125A, di/dt≤260A/μs, V_{DD}≤$V_{(BR)DSS}$，T_J ≤175°C

Test Circuit

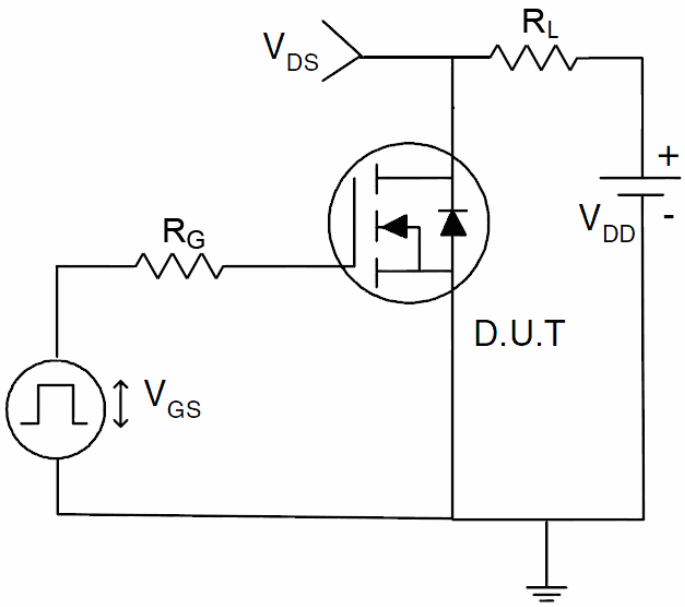
1）E_{AS} Test Circuits



2）Gate Charge Test Circuit:



3）Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics

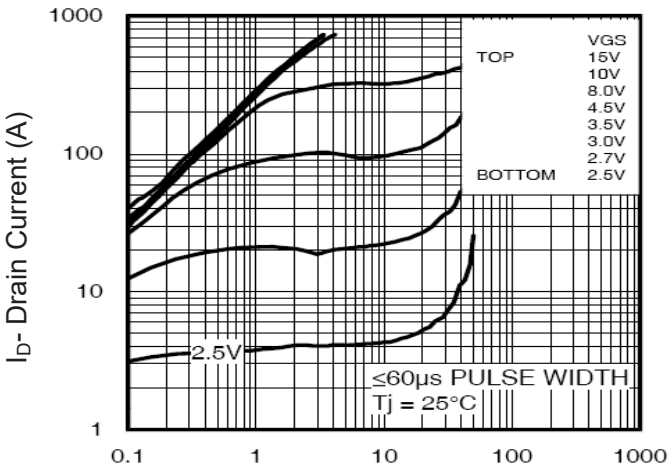


Figure 1 Output Characteristics

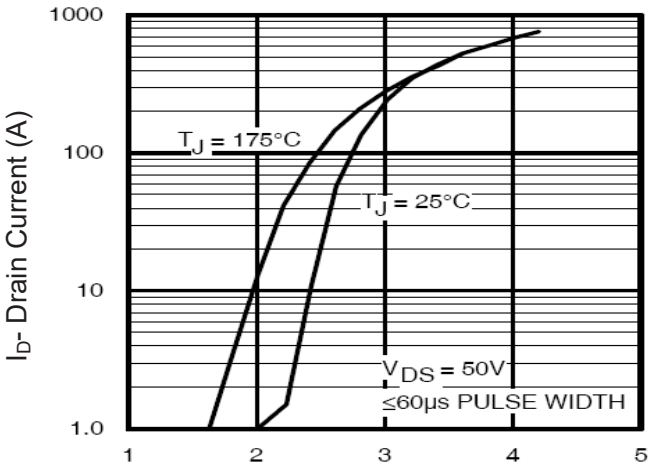


Figure 2 Transfer Characteristics

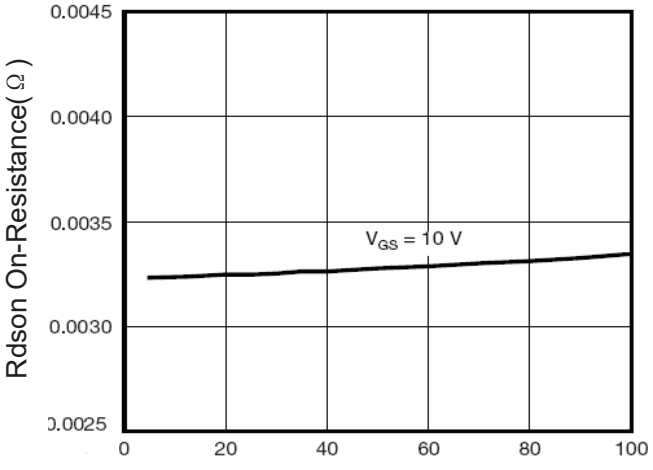


Figure 3 Rdson- Drain Current

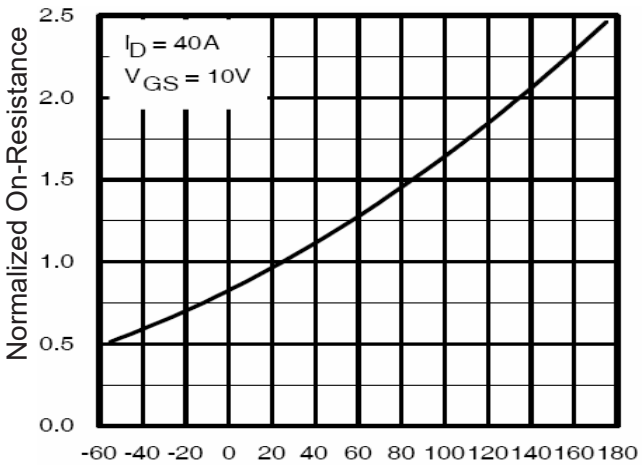


Figure 4 Rdson-JunctionTemperature

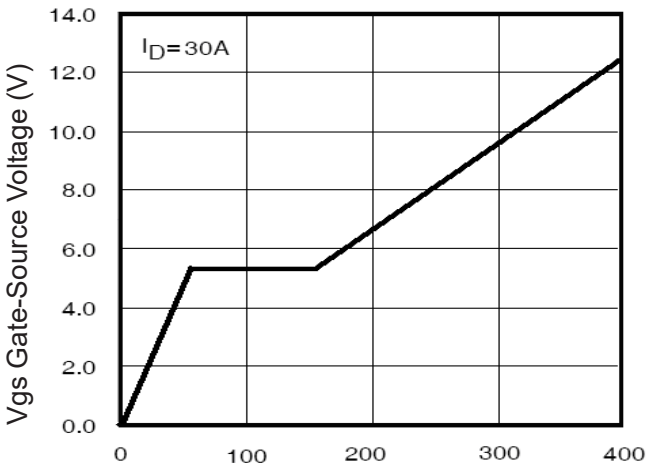


Figure 5 Gate Charge

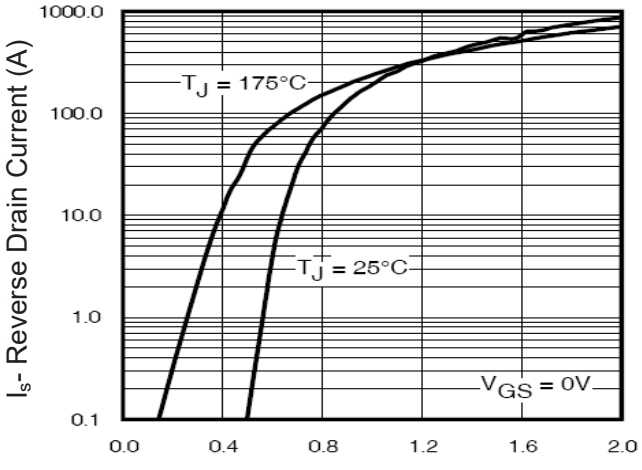


Figure 6 Source- Drain Diode Forward

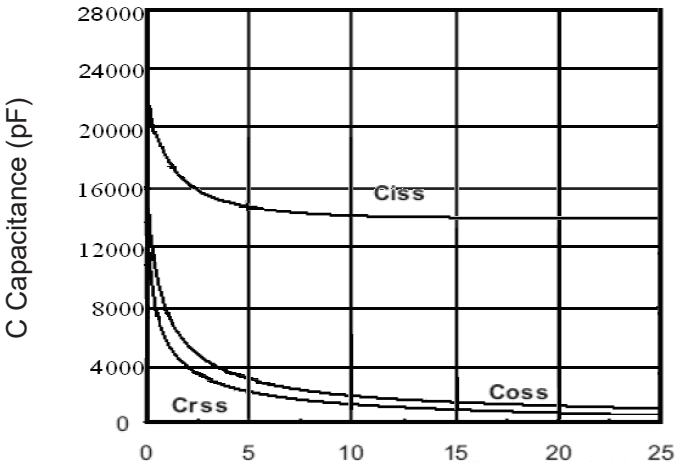


Figure 7 Capacitance vs Vds

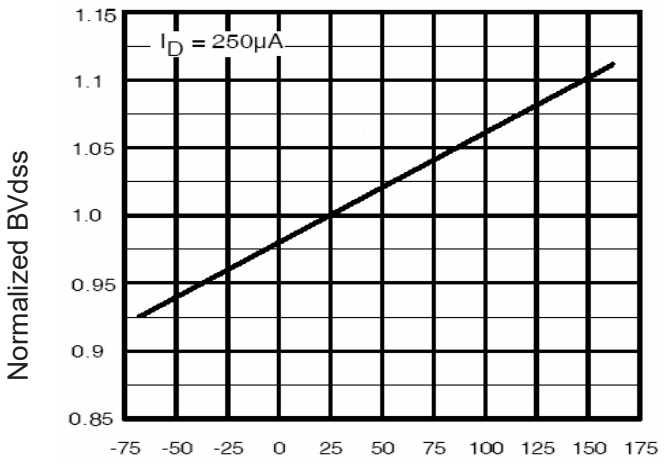


Figure 9 BV_{DSS} vs Junction Temperature

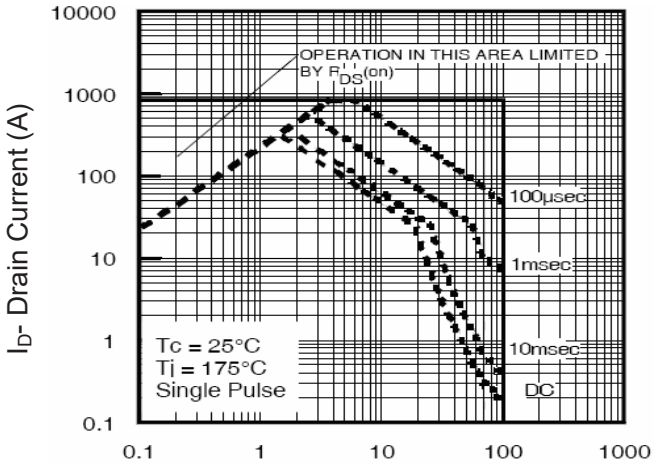


Figure 8 Safe Operation Area

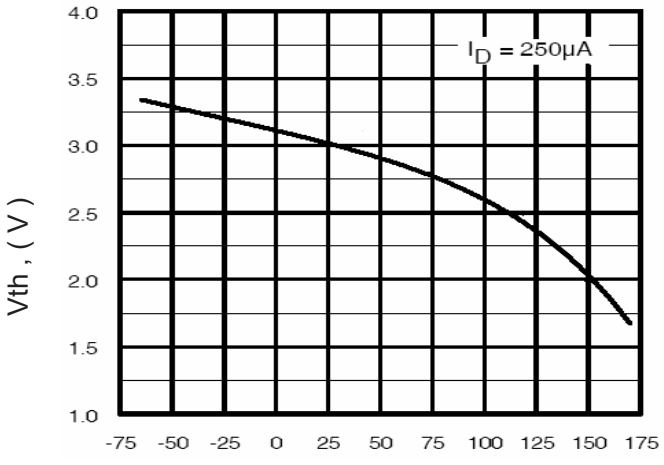


Figure 10 $V_{GS(th)}$ vs Junction Temperature

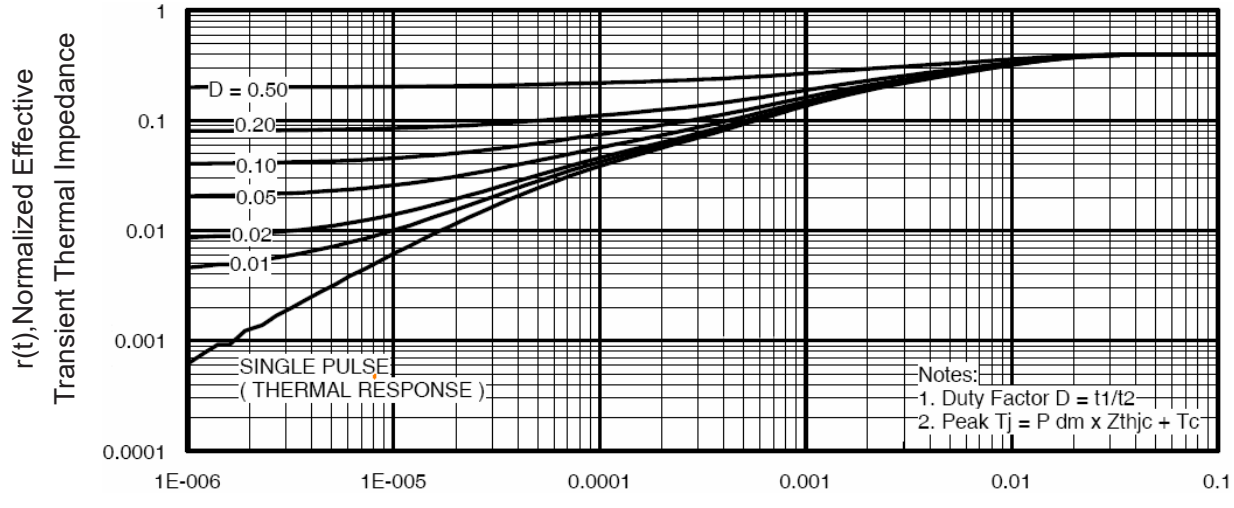


Figure 11 Normalized Maximum Transient Thermal Impedance