Description

The Power MOSFET is fabricated using the advanced planer VDMOS technology. The resulting device has low conduction resistance, superior switching performance and high avalance energy.

Features

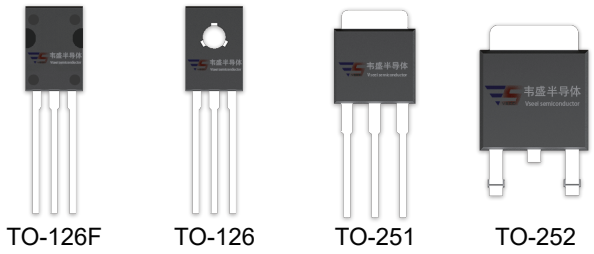
- Low $R_{DS(on)}$
- Low gate charge (typ. Q_g = 10.2 nC)
- 100% UIS tested
- RoHS compliant

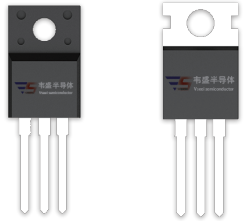
Applications

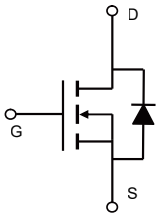
- Power factor correction.
- Switched mode power supplies.
- LED driver.

Product Summary

V_{DSS}	650V
I_D	2A
$R_{DS(on),max}$	5.2Ω
$Q_{g,typ}$	10.2 nC


TO-126F TO-126 TO-251 TO-252


TO-220F TO-220C



Schematic

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	650	V
Continuous drain current (T_C = 25°C)	I_D	2	A
(T_C = 100°C)		1.3	A
Pulsed drain current [1]	I_{DM}	8	A
Gate-Source voltage	V_{GSS}	±30	V
Avalanche energy, single pulse [2]	E_{AS}	80	mJ
Peak diode recovery dv/dt [3]	dv/dt	5	V/ns
Power Dissipation C TO-220F\TO-126(T_C = 25°C)	P_D	27	W
Derate above 25°C		0.22	W/°C
Power Dissipation C TO-220\TO-251\ TO-252 (T_C = 25°C)		35	W
Derate above 25°C		0.28	W/°C
Operating juncition and storage temperature range	T_J, T_{STG}	-55 to +150	°C
Continuous diode forward current	I_S	2	A
Diode pulse current	$I_{S,pulse}$	8	A

Thermal Characteristics

Parameter	Symbol	Value		Unit
		C TO-220F\TO-126	C TO-220\TO-251\TO-252	
Thermal resistance, Junction-to-case	$R_{\theta JC}$	4.63	3.57	°C/W
Thermal resistance, Junction-to-ambient	$R_{\theta JA}$	100	62	°C/W

Package Marking and Ordering Information

Device	Device Package	Marking	Units/Tube	Units/Reel
VSM2N65-T6F	TO-126F	VSM2N65-T6F	50	
VSM2N65-T6	TO-126	VSM2N65-T6	50	
VSM2N65-T1	TO-251	VSM2N65-T1		2500
VSM2N65-T2	TO-252	VSM2N65-T2	72	
VSM2N65-TF	TO-220F	VSM2N65-TF	50	
VSM2N65-TC	TO-220C	VSM2N65-TC	50	

Electrical Characteristics

T_c = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0 V, I_D=0.25 mA	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.25 mA	2	-	4	V
Drain cut-off current	I_{DSS}	V_{DS}=650 V, V_{GS}=0 V, T_j = 25°C T_j = 125°C	 - -	 -	 1 100	 μA
Gate leakage current, Forward	I_{GSSF}	V_{GS}=30 V, V_{DS}=0 V	-	-	100	nA
Gate leakage current, Reverse	I_{GSSR}	V_{GS}=-30 V, V_{DS}=0 V	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=1 A	-	4.2	5.2	Ω
Dynamic characteristics						
Input capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V,	-	338	-	pF
Output capacitance	C_{oss}	f = 1 MHz	-	36	-	
Reverse transfer capacitance	C_{rss}		-	3.4	-	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 325 V, I_D = 2 A	-	17.2	-	ns
Rise time	t_r	R_G = 10 Ω, V_{GS}=15 V	-	35.6	-	
Turn-off delay time	$t_{d(off)}$		-	33.9	-	
Fall time	t_f		-	29	-	
Gate charge characteristics						
Gate to source charge	Q_{gs}	V_{DD}=520 V, I_D=2 A,	-	2.6	-	nC
Gate to drain charge	Q_{gd}	V_{GS}=0 to 10 V	-	4.7	-	
Gate charge total	Q_g		-	10.2	-	
Gate plateau voltage	$V_{plateau}$		-	5	-	V
Reverse diode characteristics						
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=2 A	-	-	1.5	V
Reverse recovery time	t_{rr}	V_R=400 V, I_F=2 A,	-	221.8	-	ns
Reverse recovery charge	Q_{rr}	dI_F/dt=100 A/μs	-	0.75	-	μC
Peak reverse recovery current	I_{rrm}		-	7.4	-	A

Notes:

1. Pulse width limited by maximum junction temperature.
2. L=10mH, I_{AS} = 4A, Starting T_j= 25°C.
3. I_{SD} = 2A, di/dt≤100A/us, V_{DD}≤BV_{DS}, Starting T_j= 25°C.

Electrical Characteristics Diagrams

Figure 1. Typical Output Characteristics

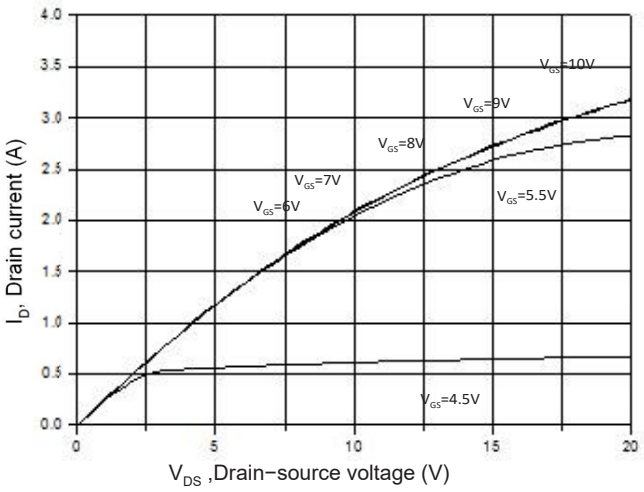


Figure 2. Transfer Characteristics

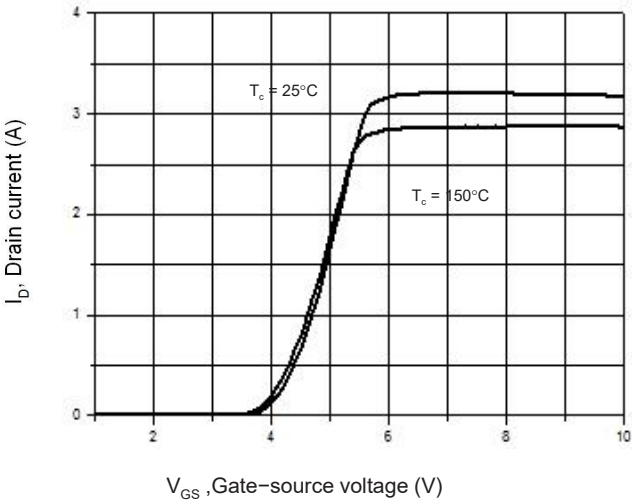


Figure 3. On-Resistance Variation vs. Drain Current

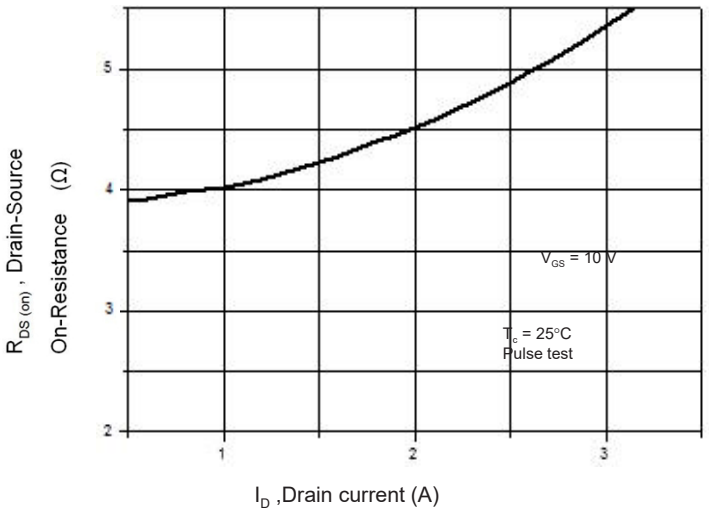


Figure 4. Threshold Voltage vs. Temperature

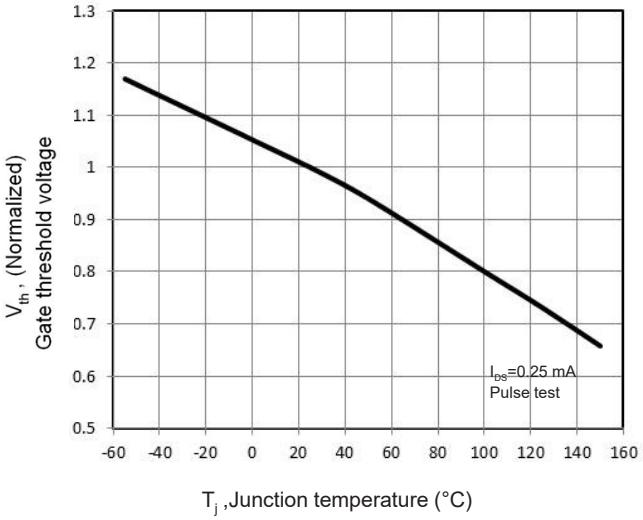


Figure 5. Breakdown Voltage vs. Temperature

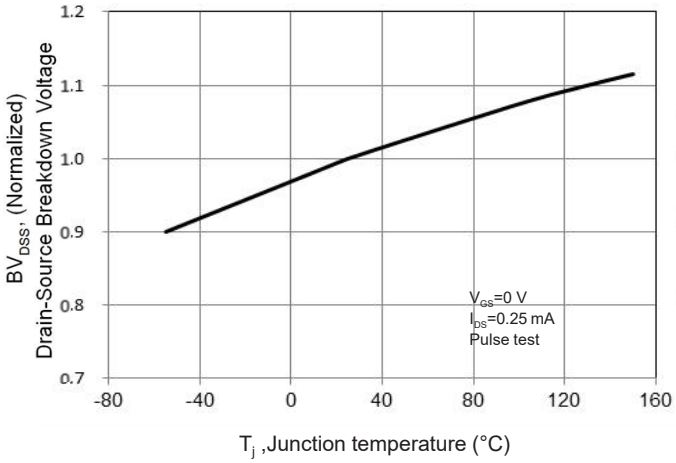


Figure 6. On-Resistance vs. Temperature

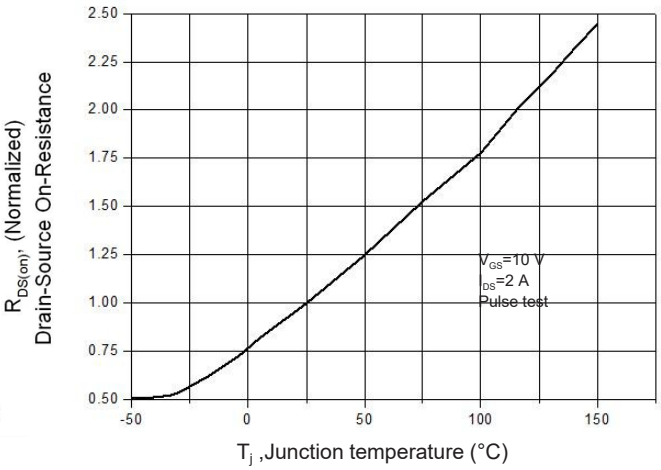


Figure 7. Capacitance Characteristics

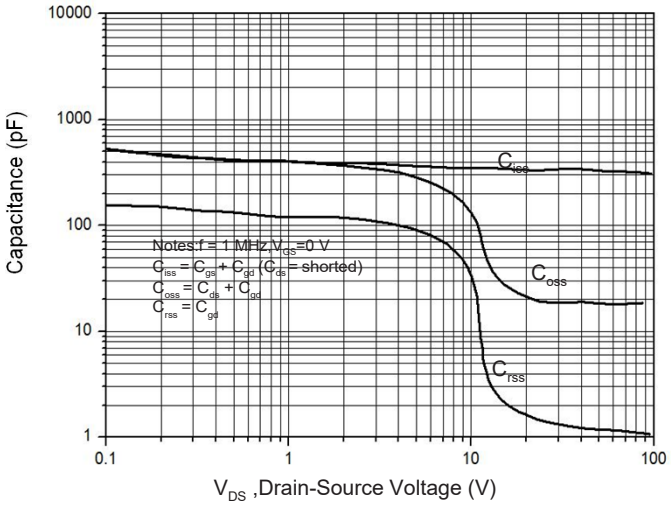


Figure 8. Gate Charge Characterist

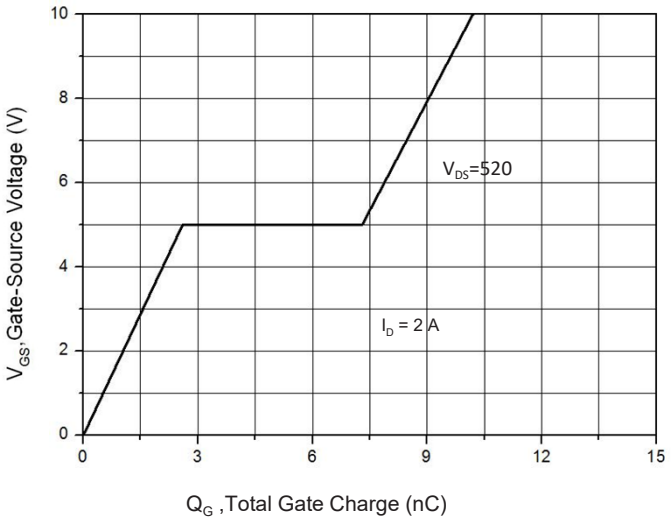


Figure 9. Maximum Safe Operating Area

C C TO-220F

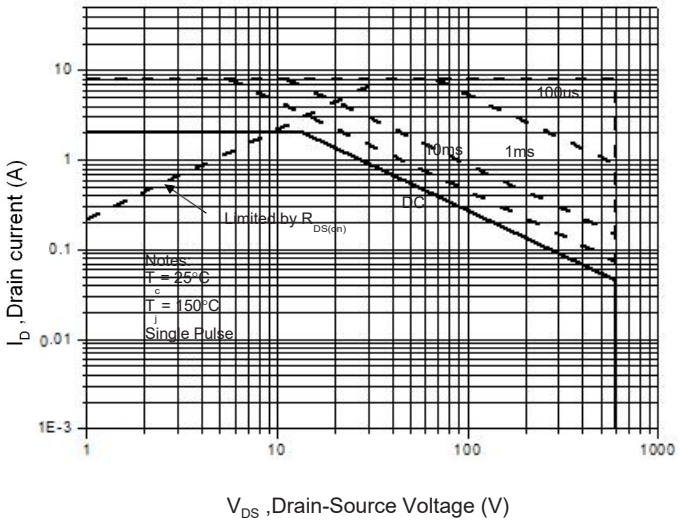


Figure 10. Maximum Safe Operating Area

C C TO-220/TO-251/TO-252

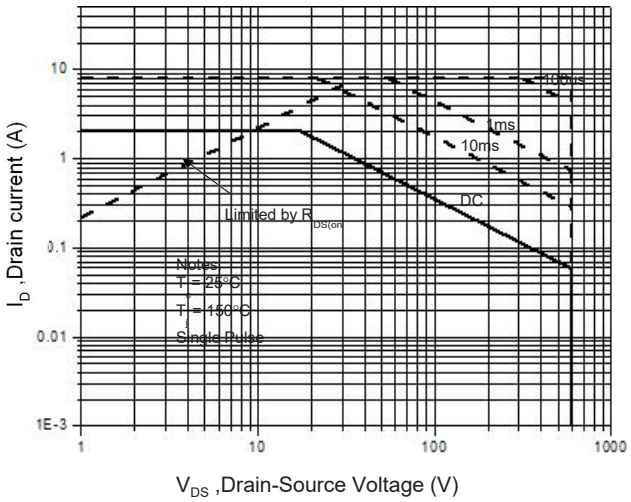


Figure 11. Power Dissipation vs. Temperature

C C TO-220F/TO-126

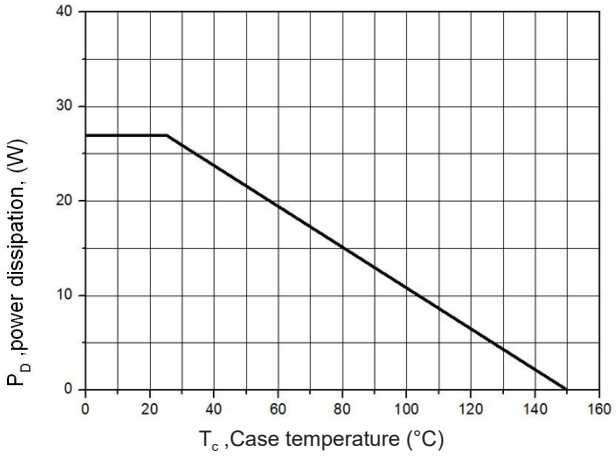


Figure 12. Power Dissipation vs. Temperature

C C TO-220/TO-251/TO-252

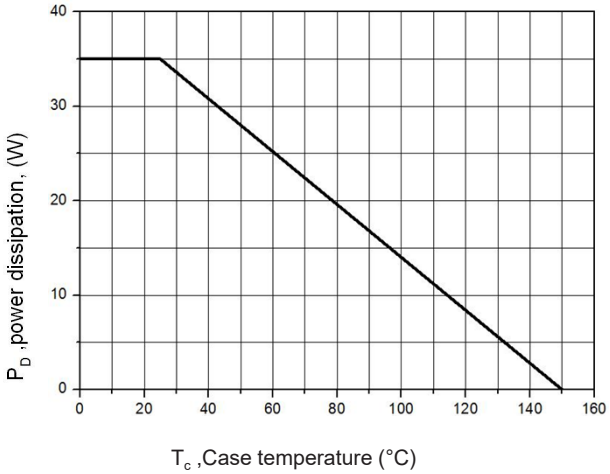


Figure 13. Continuous Drain Current vs. Temperature

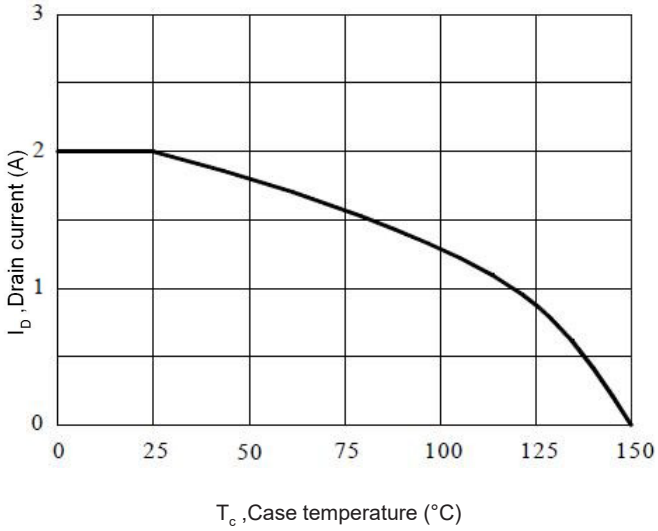


Figure 14. Body Diode Transfer Characteristics

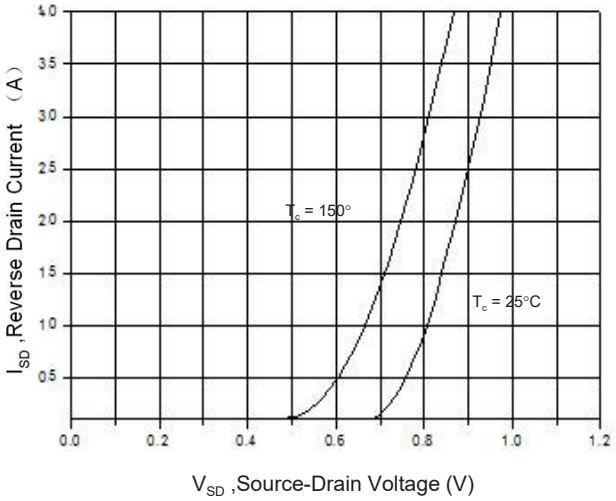


Figure 15 Transient Thermal Impendance,Junction to Case，C TO-220F/TO-126

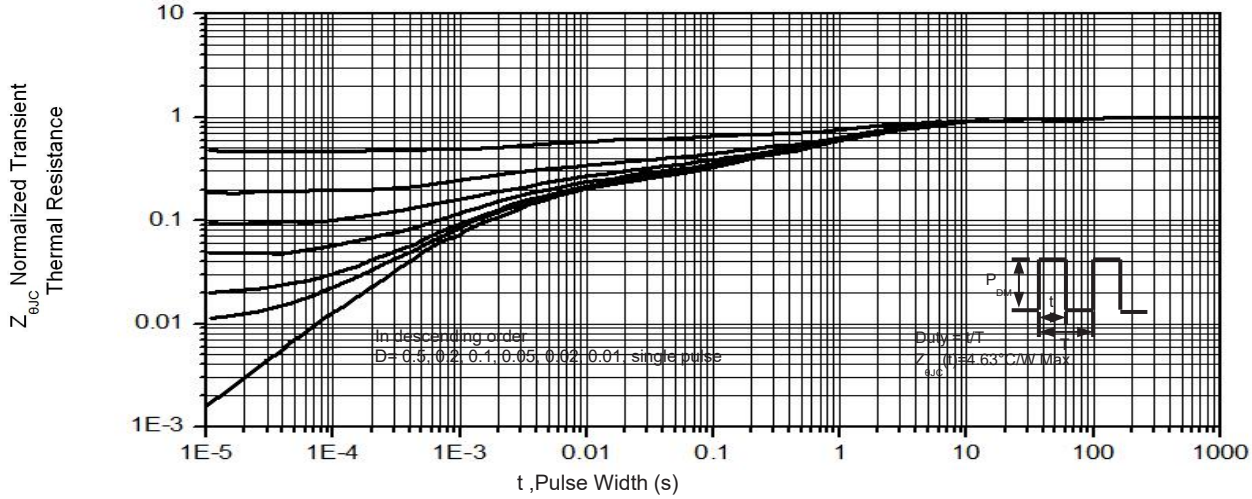
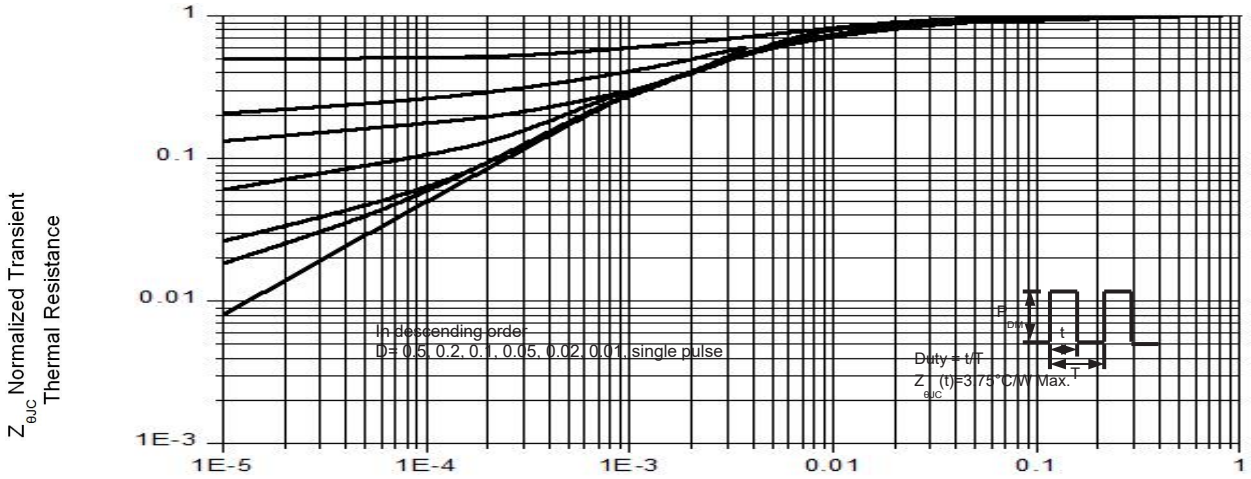
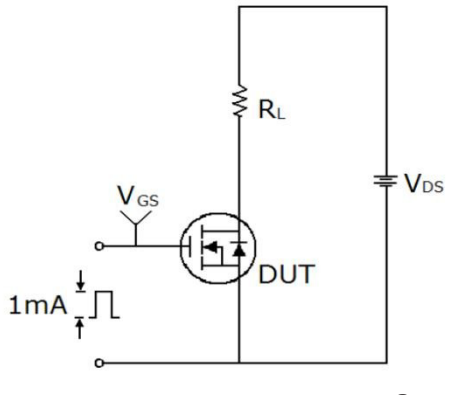
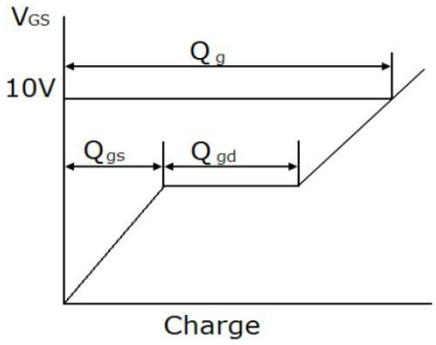


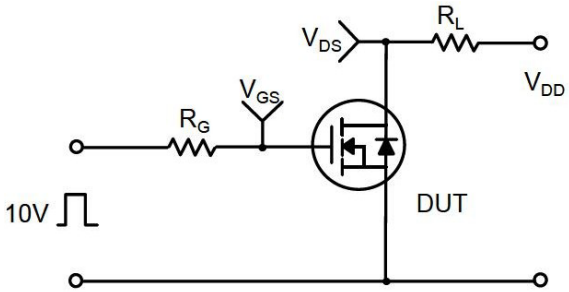
Figure 16. Transient Thermal Impendance,Junction to Case，C TO-220/TO-251/TO-252

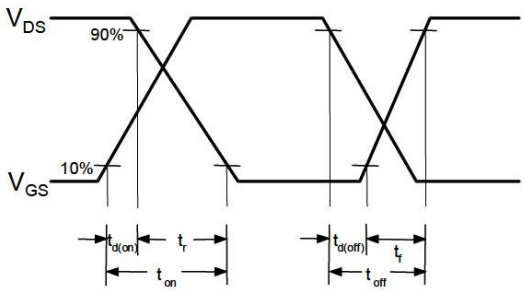


Gate Charge Test Circuit & Waveform









Unclamped Inductive Switching Test Circuit & Waveforms