

### Description

The VSM30P10 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications. It is ESD protected.

### General Features

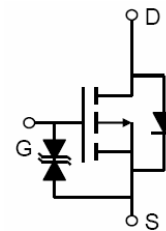
- $V_{DS} = -100V, I_D = -30A$   
 $R_{DS(ON)} < 58m\Omega @ V_{GS} = -10V$  (Typ:50m $\Omega$ )
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density cell design for ultra low On-Resistance

### Application

- Portable equipment and battery powered systems



TO-220C



Schematic Diagram

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM30P10-TC	VSM30P10	TO-220C	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-30	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	-21	A
Pulsed Drain Current	$I_{DM}$	-120	A
Maximum Power Dissipation	$P_D$	120	W
Derating factor		0.8	W/ $^\circ C$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

**Thermal Characteristic**

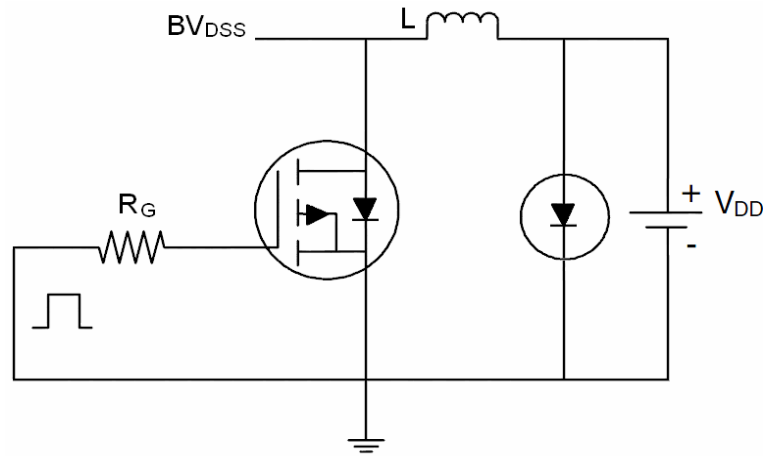
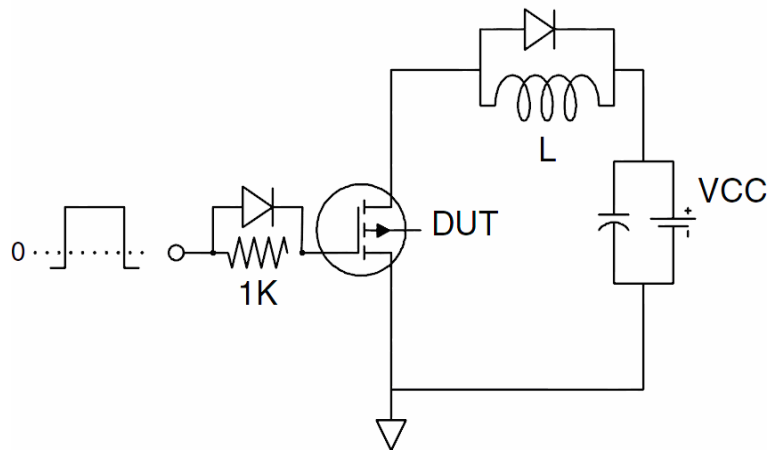
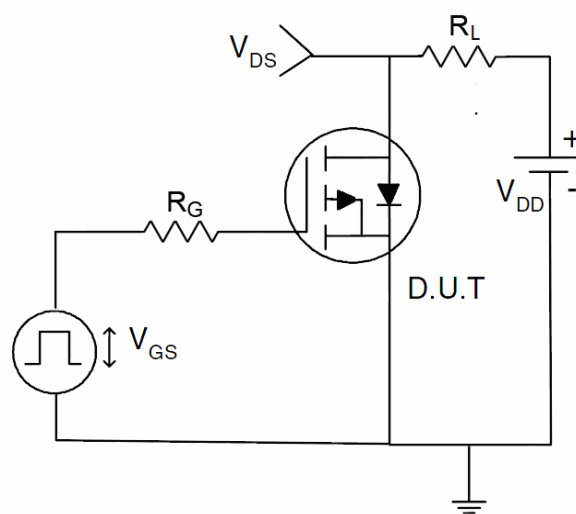
Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta Jc}$	1.25	$^{\circ}\text{C/W}$
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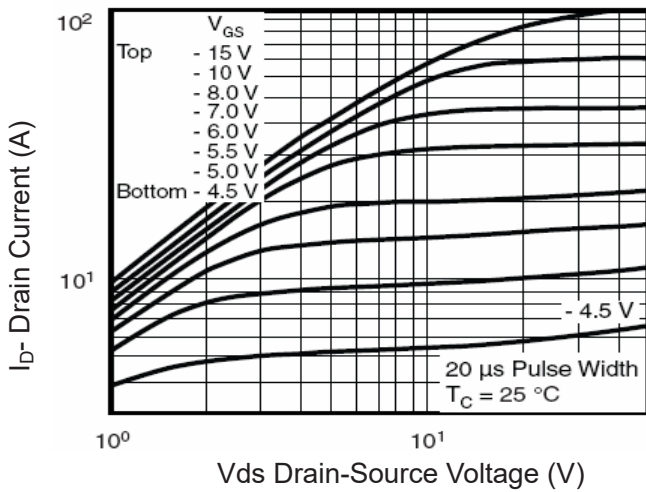
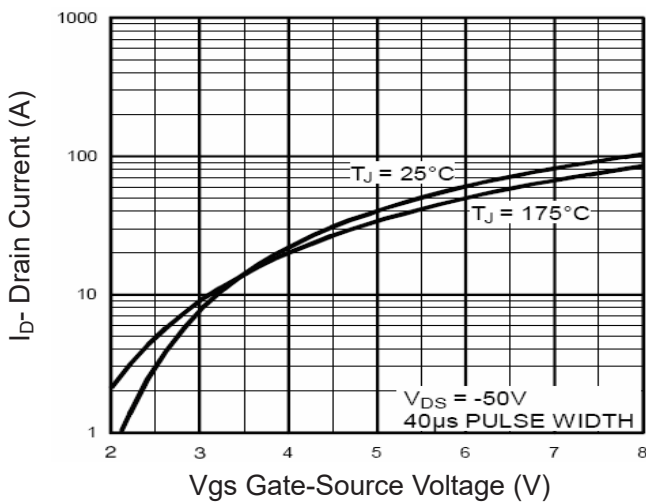
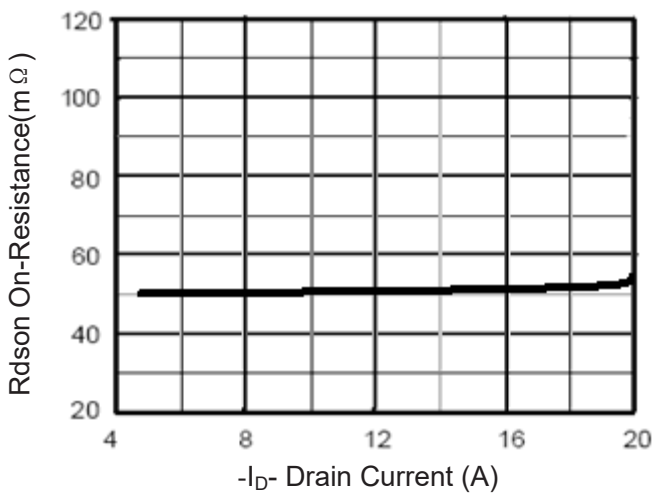
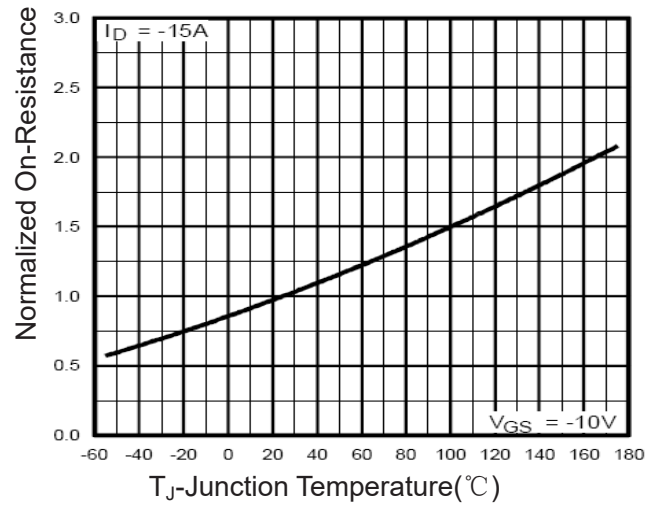
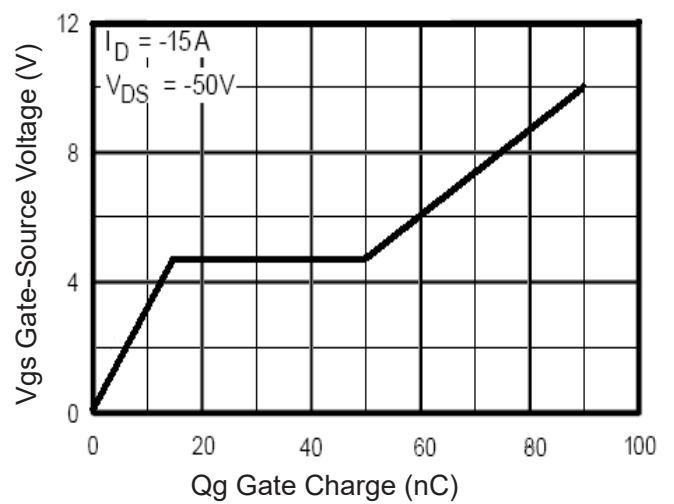
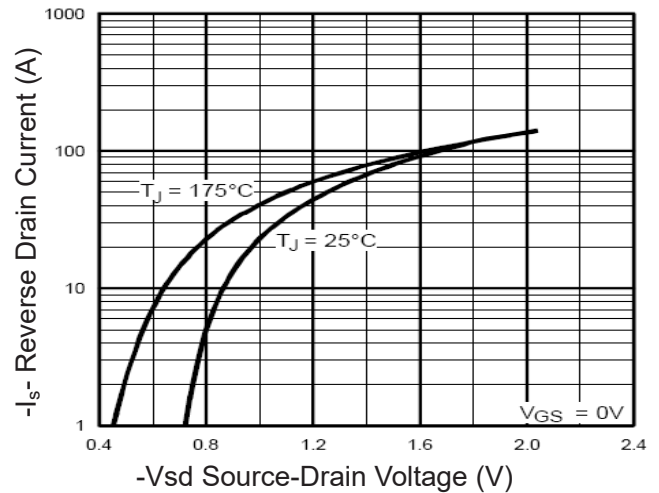
**Electrical Characteristics ( $T_c=25^{\circ}\text{C}$  unless otherwise noted)**

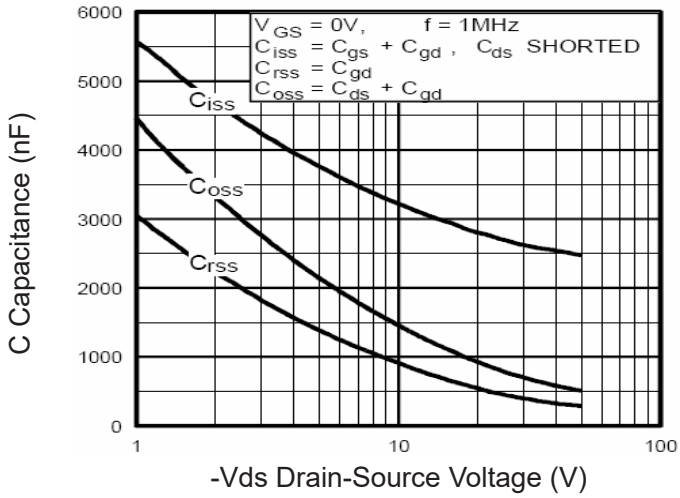
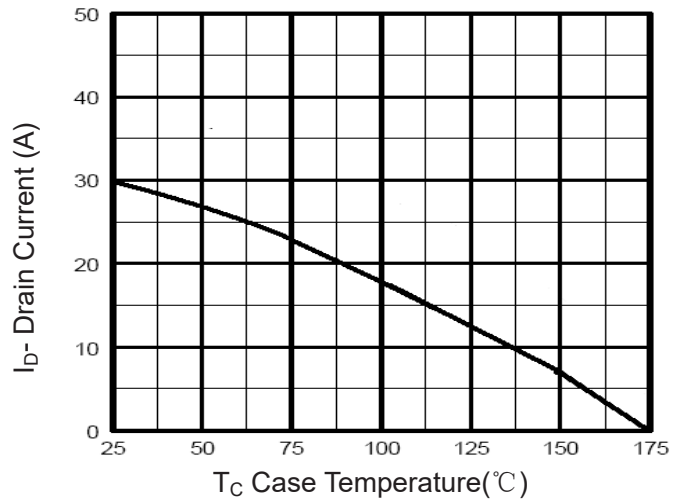
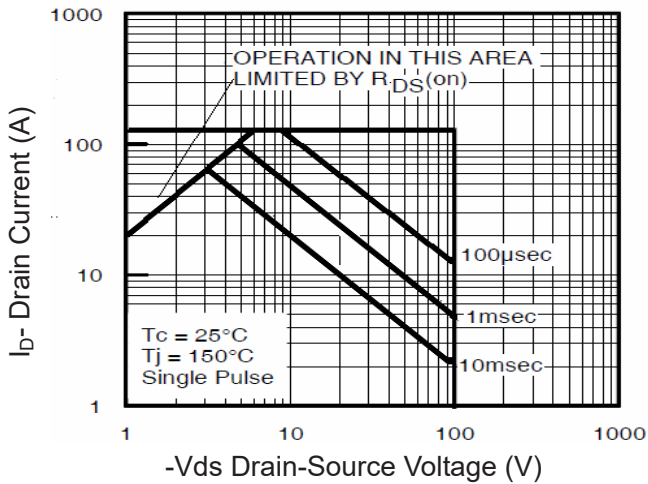
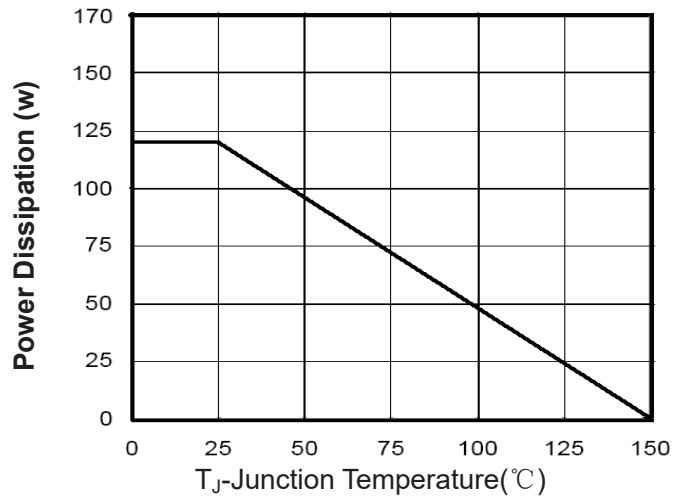
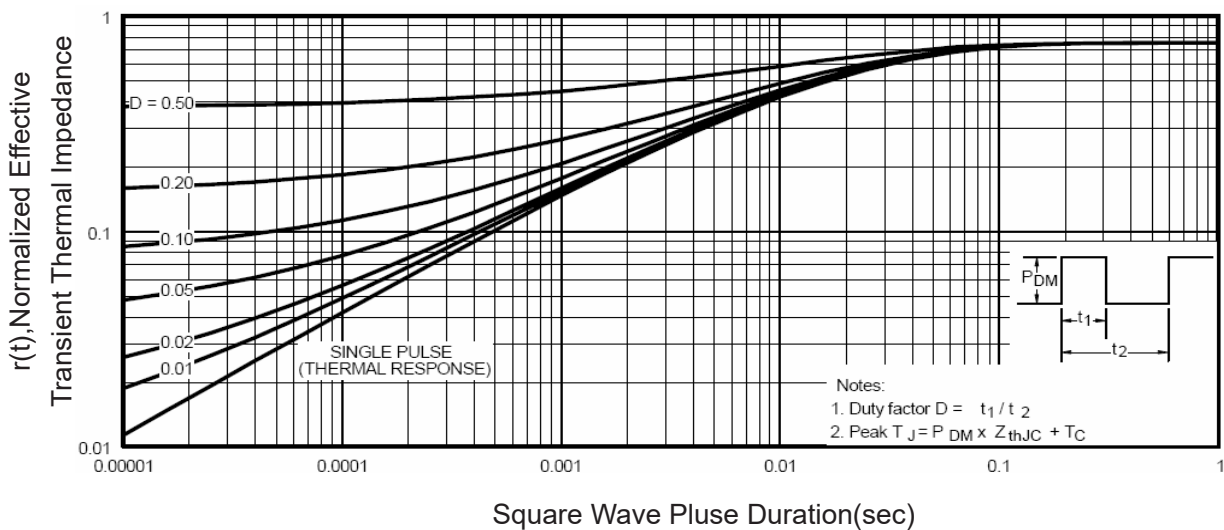
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-100	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-100V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 10$	$\mu A$
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.5	-1.9	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-15A$	-	50	58	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-50V, I_D=-10A$	5	-	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{ISS}$	$V_{DS}=-25V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	2700	-	PF
Output Capacitance	$C_{OSS}$		-	790	-	PF
Reverse Transfer Capacitance	$C_{RSS}$		-	450	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-50V, I_D=-15A$ $V_{GS}=-10V, R_{GEN}=9.1\Omega$	-	17	-	nS
Turn-on Rise Time	$t_r$		-	80	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	45	-	nS
Turn-Off Fall Time	$t_f$		-	65	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-50V, I_D=-15A,$ $V_{GS}=-10V$	-	90	-	nC
Gate-Source Charge	$Q_{gs}$		-	15	-	nC
Gate-Drain Charge	$Q_{gd}$		-	35	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=-10A$	-	-	-1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$	-	-	-	-30	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}, I_F = -15A$ $di/dt = 100A/\mu s$ <sup>(Note 3)</sup>	-	90	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	70	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^{\circ}\text{C}, V_{DD}=-50V, V_G=-10V, L=0.5\text{mH}, R_g=25\Omega$

**Test Circuit**
**1) E<sub>AS</sub> Test Circuit**

**2) Gate Charge Test Circuit**

**3) Switch Time Test Circuit**


**Typical Electrical and Thermal Characteristics (Curves)**

**Figure 1 Output Characteristics**

**Figure 2 Transfer Characteristics**

**Figure 3  $R_{DS(on)}$ - Drain Current**

**Figure 4  $R_{DS(on)}$ -Junction Temperature**

**Figure 5 Gate Charge**

**Figure 6 Source- Drain Diode Forward**


**Figure 7 Capacitance vs Vds**

**Figure 9 Drain Current vs Case Temperature**

**Figure 8 Safe Operation Area**

**Figure 10 Power De-rating**

**Figure 11 Normalized Maximum Transient Thermal Impedance**