## Description

The VSM3N20 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

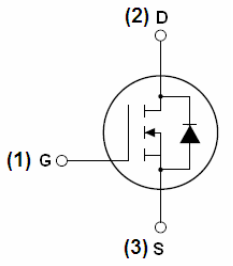
## General Features

- $V_{DS}$ =200V,$I_D$ =3.9A
  $R_{DS(ON)}$ < 79mΩ @ $V_{GS}$=10V （Typ：56mΩ）
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Low gate to drain charge to reduce switching losses

## Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply


SOP-8




Schematic Diagram

## Package Marking and Ordering Information

| Device Marking | Device | Device Package | Reel Size | Tape width | Quantity |
|---|---|---|---|---|---|
| VSM3N20-S8 | VSM3N20 | SOP-8 | Ø330mm | 12mm | 2500 units |

## Absolute Maximum Ratings ($T_A$=25℃unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 200 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Drain Current-Continuous | $I_D$ | 3.9 | A |
| Drain Current-Continuous($T_C$=100℃) | $I_D$ (100℃) | 2.8 | A |
| Pulsed Drain Current | $I_{DM}$ | 30 | A |
| Maximum Power Dissipation | $P_D$ | 3 | W |
| Operating Junction and Storage Temperature Range | $T_J$,$T_{STG}$ | -55 To 150 | ℃ |

## Thermal Characteristic

| | | | |
|---|---|---|---|
| Thermal Resistance,Junction-to-Case(Note 2) | $R_{\theta JC}$ | 41.7 | ℃/W |

## Electrical Characteristics ($T_A$=25℃unless otherwise noted)

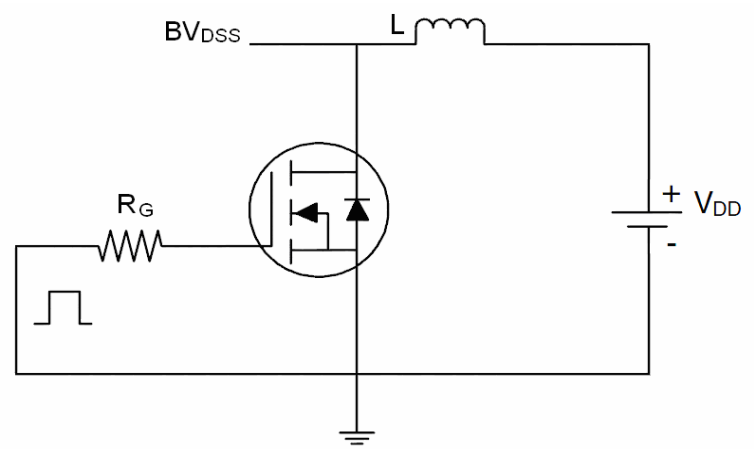
| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V $I_D$=250μA | 200 | 215 | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=200V,$V_{GS}$=0V | - | - | 1 | μA |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V,$V_{DS}$=0V | - | - | ±100 | nA |
| **On Characteristics** (Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,$I_D$=250μA | 2 | 3 | 4 | V |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=3.7A | - | 56 | 79 | mΩ |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$=50V,$I_D$=3.9A | 7 | - | - | S |
| **Dynamic Characteristics** (Note4) | | | | | | |
| Input Capacitance | $C_{lss}$ | $V_{DS}$=25V,$V_{GS}$=0V, F=1.0MHz | | 4200 | | PF |
| Output Capacitance | $C_{oss}$ | | | 163 | | PF |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 75 | | PF |
| **Switching Characteristics** (Note 4) | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$=100V,$I_D$=2.2A $V_{GS}$=10V,$R_{GEN}$=6.5Ω | - | 15 | - | nS |
| Turn-on Rise Time | $t_r$ | | - | 13 | - | nS |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 26 | - | nS |
| Turn-Off Fall Time | $t_f$ | | - | 14 | - | nS |
| Total Gate Charge | $Q_g$ | $V_{DS}$=100V,$I_D$=2.2A, $V_{GS}$=10V | - | 38 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 9 | - | nC |
| Gate-Drain Charge | $Q_{gd}$ | | - | 15 | - | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| Diode Forward Voltage (Note 3) | $V_{SD}$ | $V_{GS}$=0V,$I_S$=3.7A | - | - | 1.2 | V |
| Diode Forward Current (Note 2) | $I_S$ | | - | - | 3.9 | A |

## Notes:

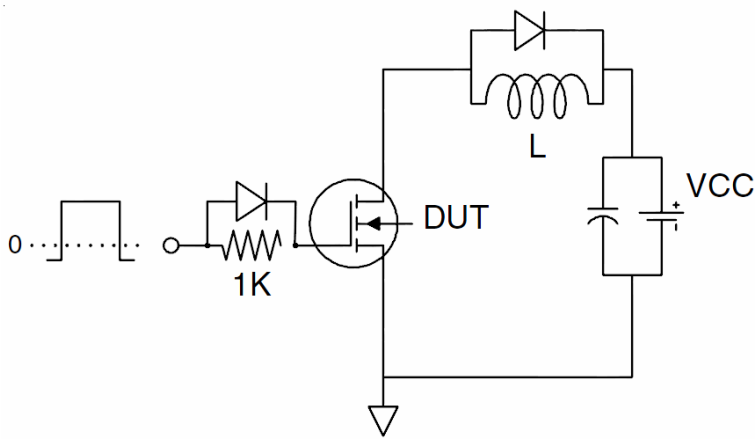
**1.** Repetitive Rating: Pulse width limited by maximum junction temperature.
**2.** Surface Mounted on FR4 Board, t ≤ 10 sec.
**3.** Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
**4.** Guaranteed by design, not subject to production

## Test Circuit

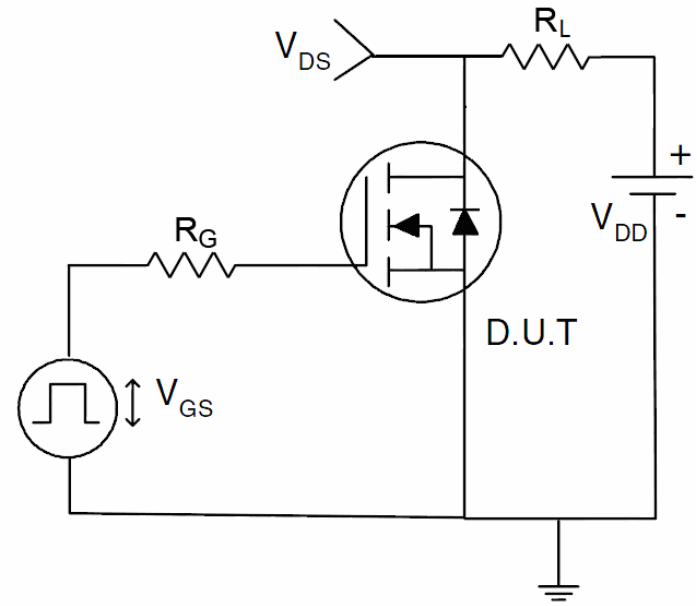
### 1）$E_{AS}$ test Circuit




### 2）Gate charge test Circuit




### 3）Switch Time Test Circuit



## Typical Electrical and Thermal Characteristics (Curves)

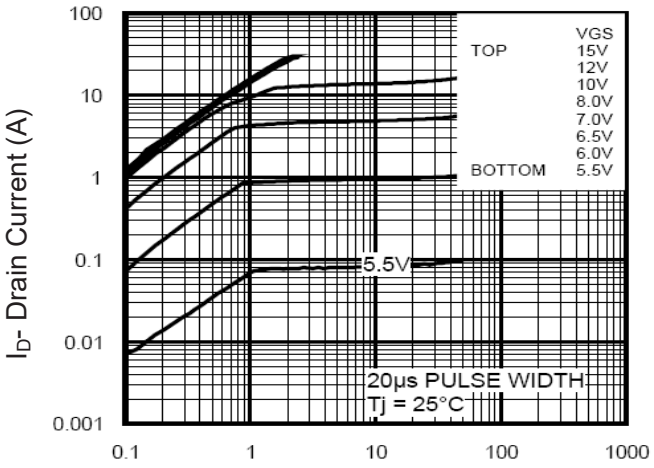



**Figure 1 Output Characteristics**

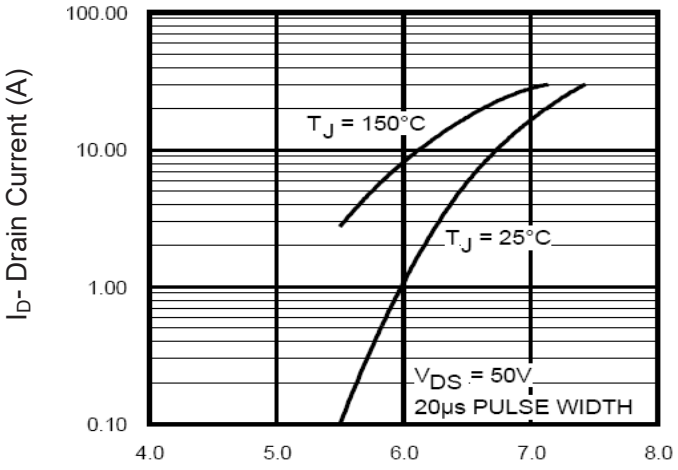



**Figure 2 Transfer Characteristics**

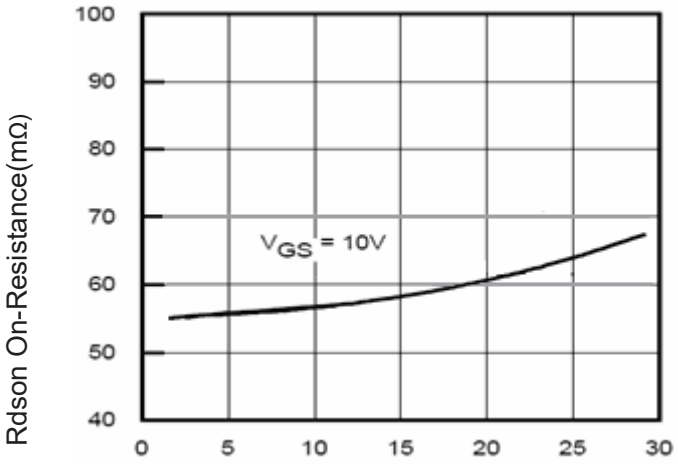



**Figure 3 Rdson- Drain Current**

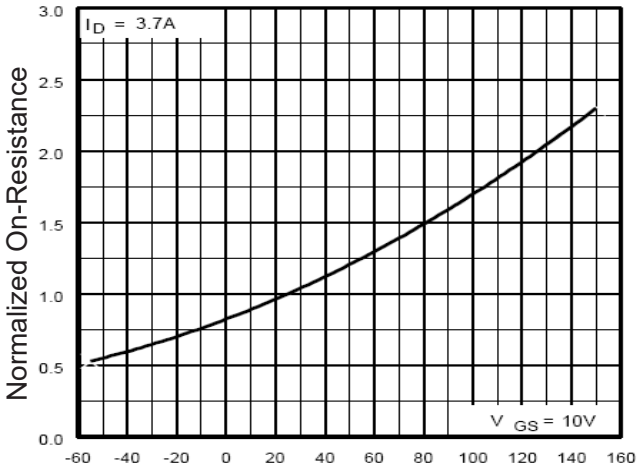



**Figure 4 Rdson-JunctionTemperature**

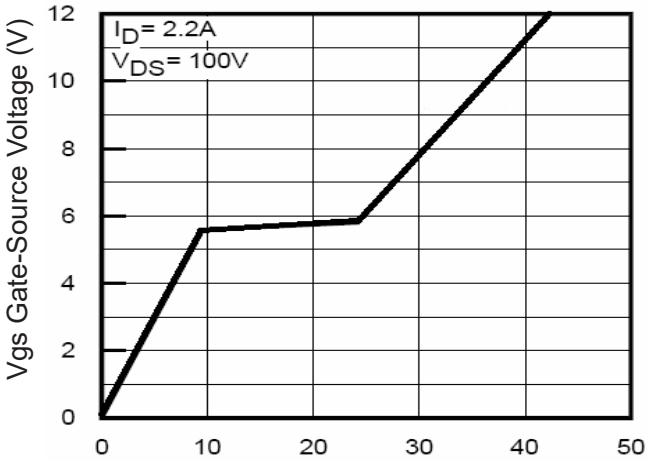



**Figure 5 Gate Charge**

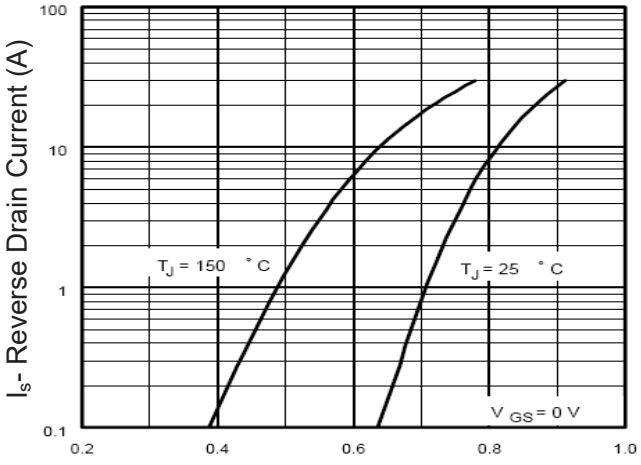



**Figure 6 Source- Drain Diode Forward**

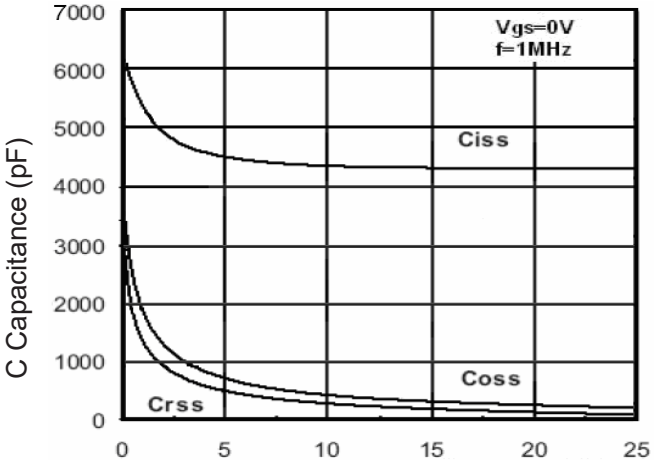



**Figure 7 Capacitance vs Vds**

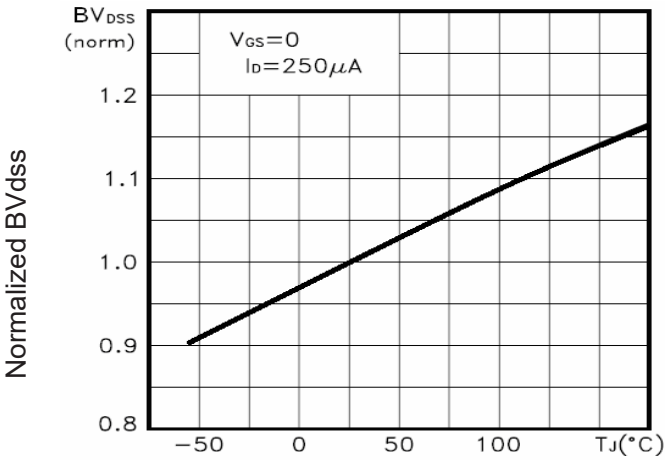



**Figure 9 $BV_{DSS}$ vs Junction Temperature**

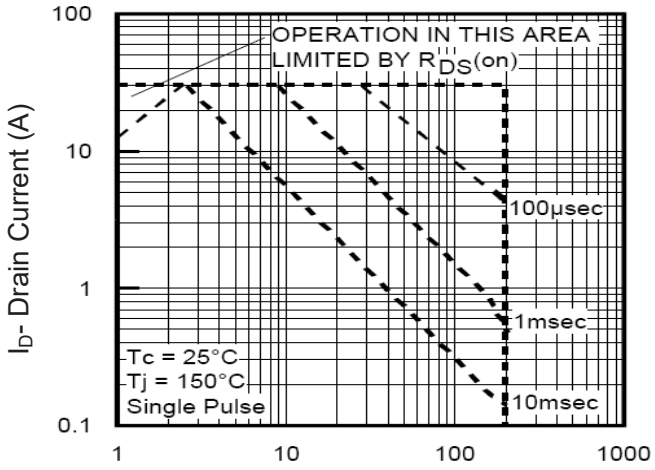



**Figure 8 Safe Operation Area**

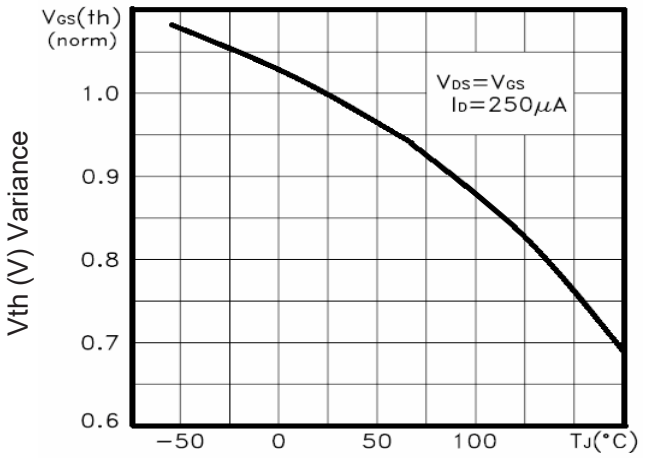



**Figure 10 $V_{GS(th)}$ vs Junction Temperature**

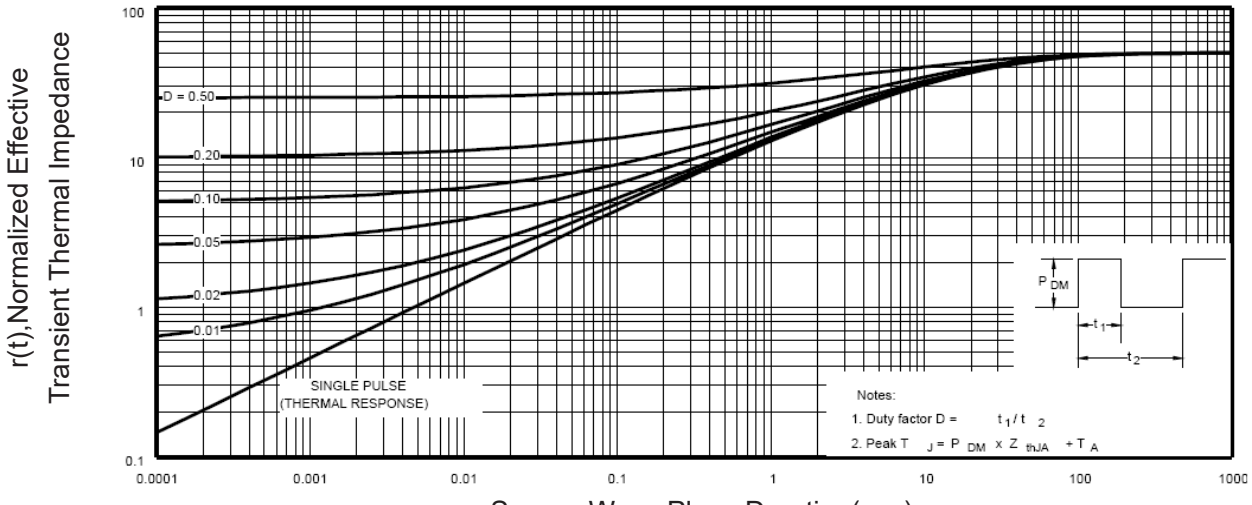



**Figure 11 Normalized Maximum Transient Thermal Impedance**