Description

The VSM40N15 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

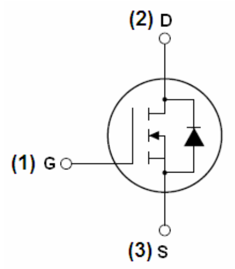
General Features

- V_{DS} =150V,I_D =40A
  $R_{DS(ON)}$ < 45mΩ @ V_{GS}=10V (Typ:35mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

TO-252



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM40N15-T2	VSM40N15	TO-252	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	40	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	29	A
Pulsed Drain Current	I_{DM}	160	A
Maximum Power Dissipation	P_D	140	W
Derating factor		0.93	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	350	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	1.07	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

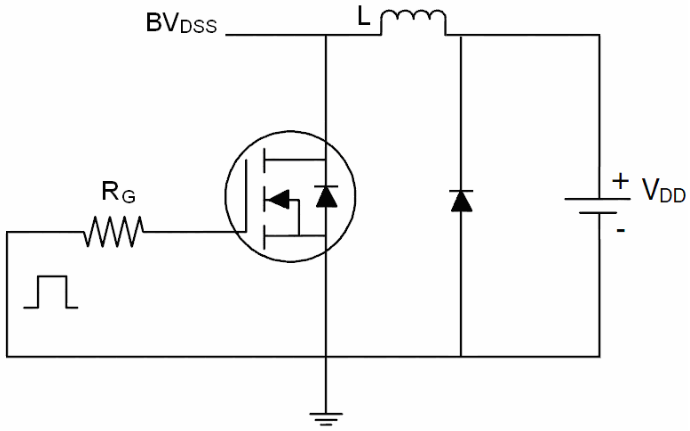
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	150	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±12V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	0.7	1.05	1.4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=18A	-	35	45	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=18A	38	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=75V,V_{GS}=0V, F=1.0MHz	-	4300	-	PF
Output Capacitance	C_{oss}		-	130	-	PF
Reverse Transfer Capacitance	C_{rss}		-	111	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V,I_D=2A,R_L=15Ω V_{GS}=10V,R_G=2.5Ω	-	14	-	nS
Turn-on Rise Time	t_r		-	12	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	45	-	nS
Turn-Off Fall Time	t_f		-	11	-	nS
Total Gate Charge	Q_g	V_{DS}=75V,I_D=18A, V_{GS}=4.5V		63.8	-	nC
Gate-Source Charge	Q_{gs}			9.8	-	nC
Gate-Drain Charge	Q_{gd}			26.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=18A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	40	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 18A di/dt = 100A/μs(Note3)	-	42	-	nS
Reverse Recovery Charge	Qrr		-	75	-	nC

Notes:

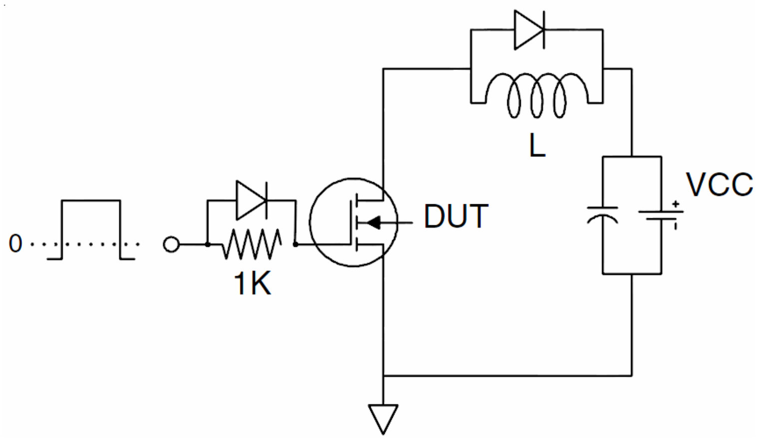
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition:Tj=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω

Test Circuit

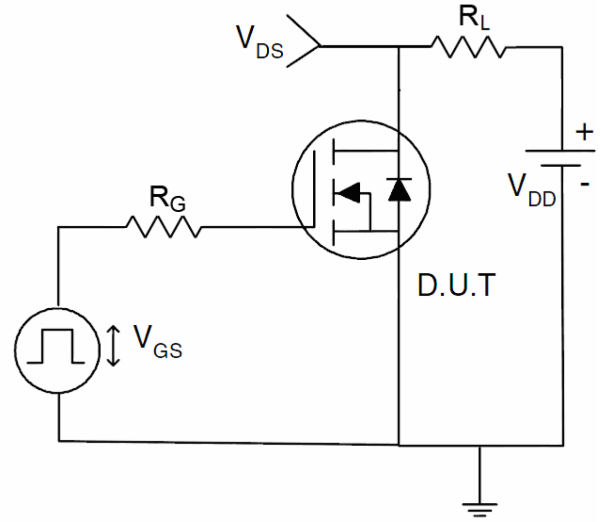
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

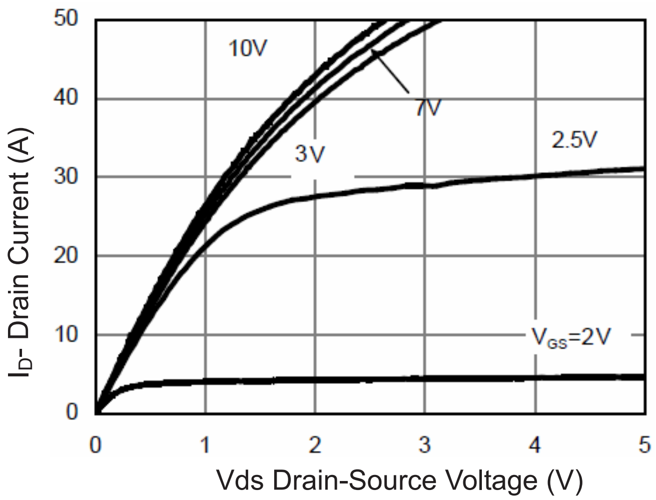


Figure 1 Output Characteristics

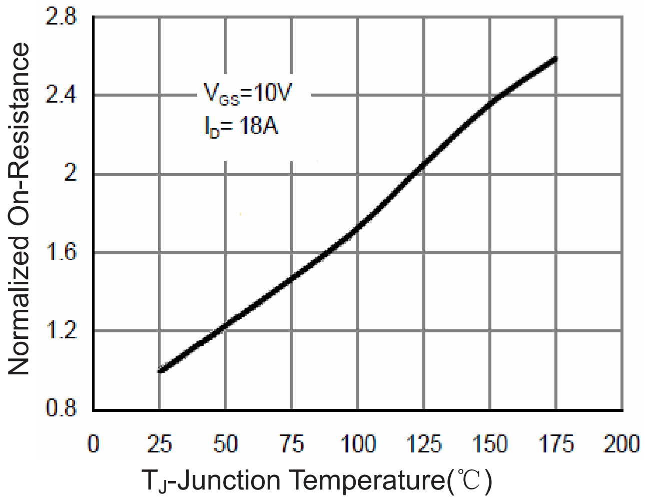


Figure 4 Rdson-JunctionTemperature

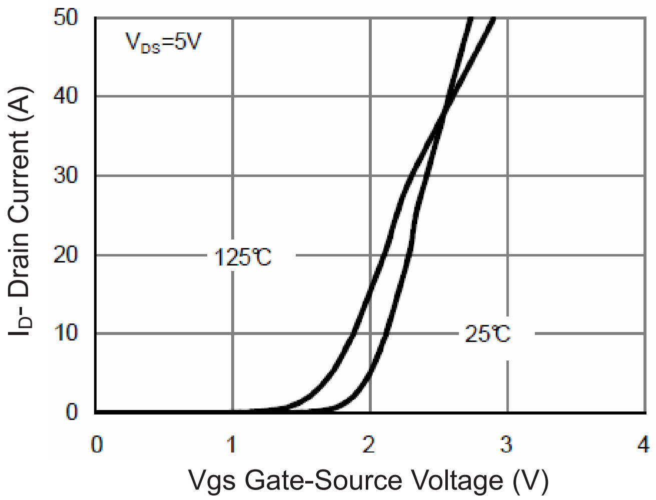


Figure 2 Transfer Characteristics

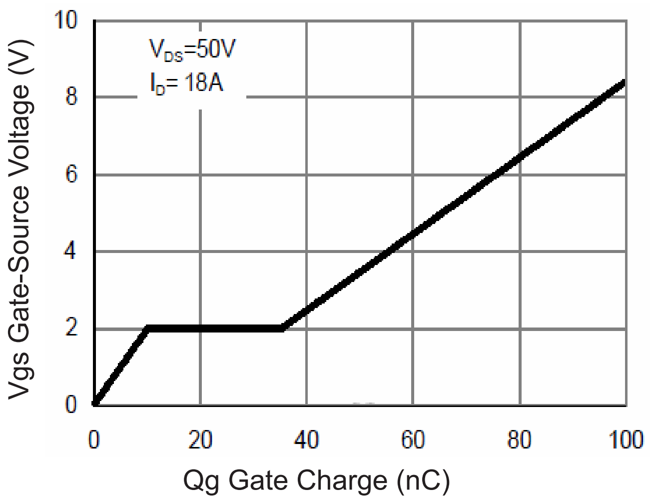


Figure 5 Gate Charge

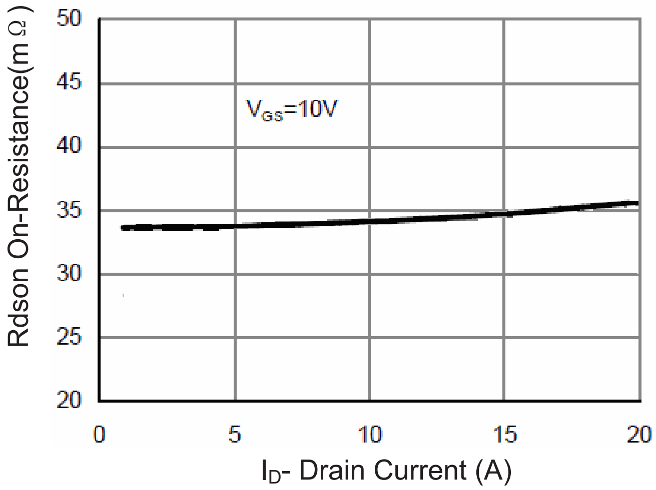


Figure 3 Rdson- Drain Current

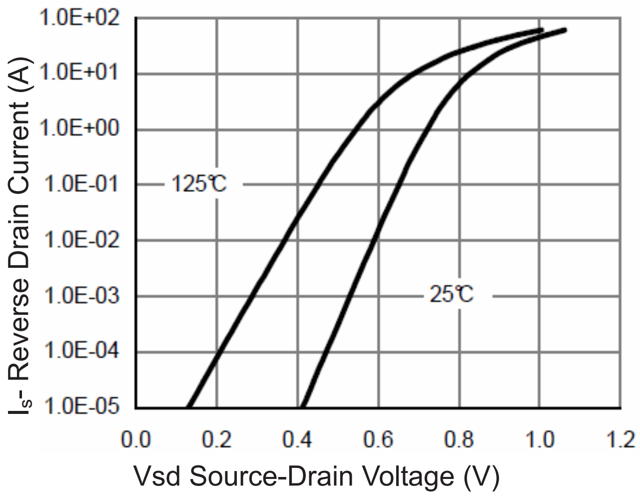


Figure 6 Source- Drain Diode Forward

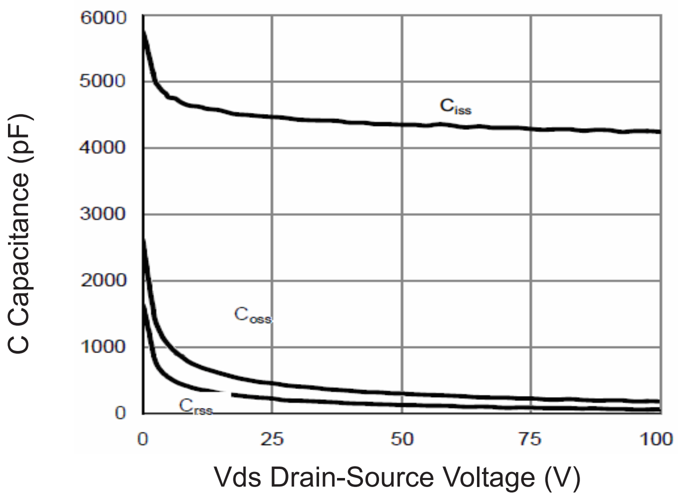


Figure 7 Capacitance vs Vds

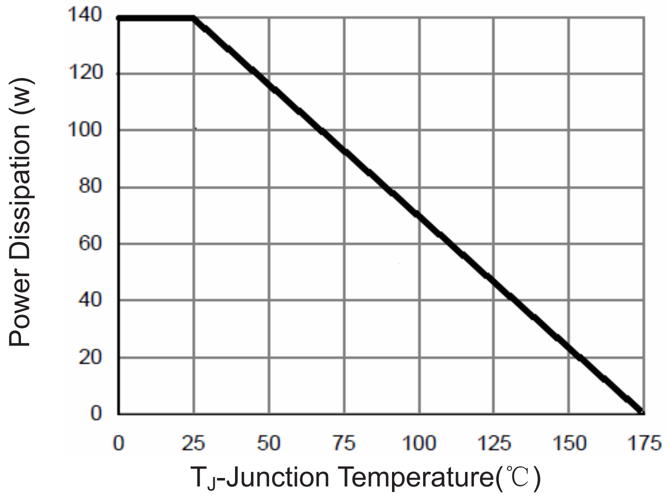


Figure 9 Power De-rating

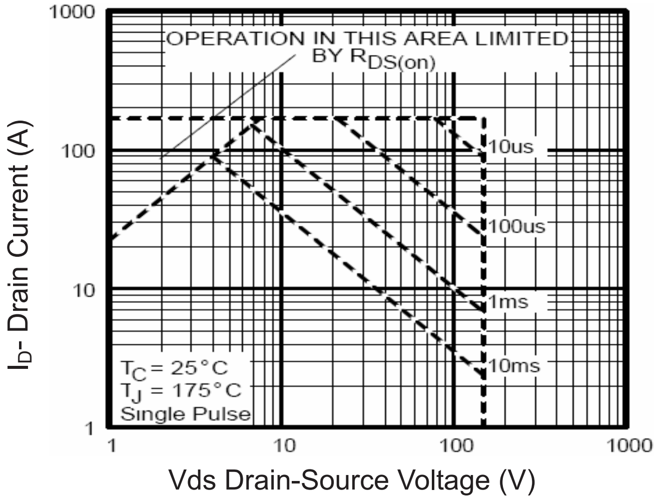


Figure 8 Safe Operation Area

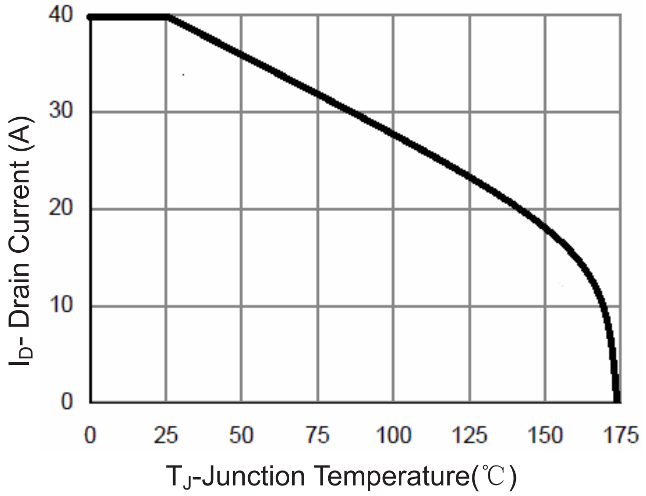


Figure 10 Current De-rating

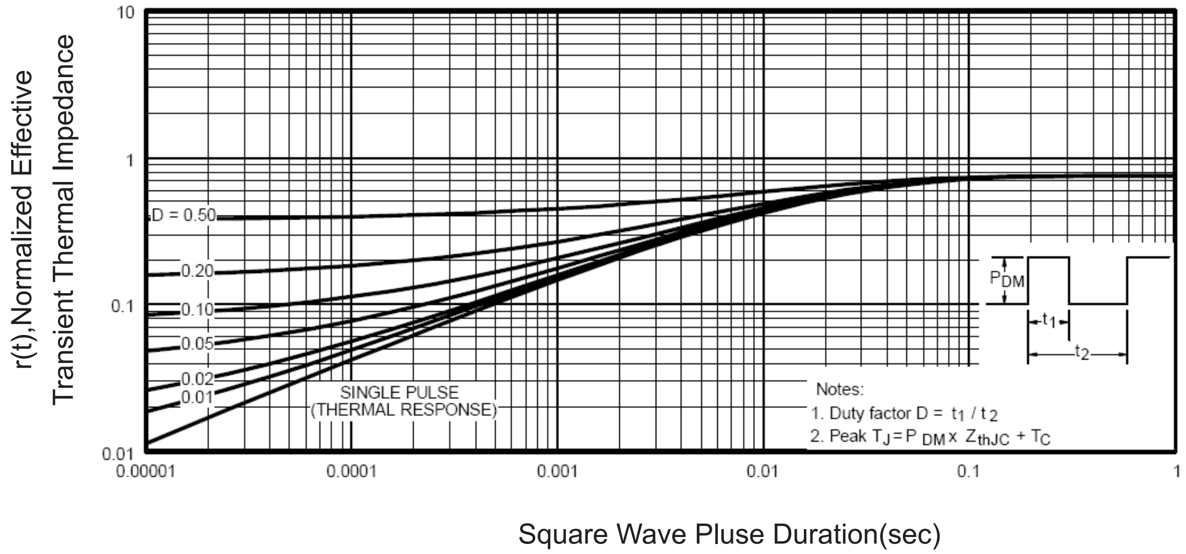


Figure 11 Normalized Maximum Transient Thermal Impedance