

Description

The VSM40N20 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

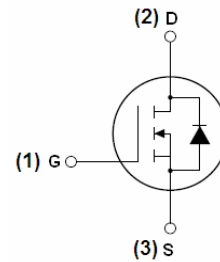
- $V_{DS} = 200V, I_D = 40A$
 $R_{DS(ON)} < 41m\Omega @ V_{GS} = 10V$
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



TO-220C



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM40N20-TC	VSM40N20	TO-220C	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	40	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	28	A
Pulsed Drain Current	I_{DM}	160	A
Maximum Power Dissipation	P_D	220	W
Derating factor		1.47	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	480	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

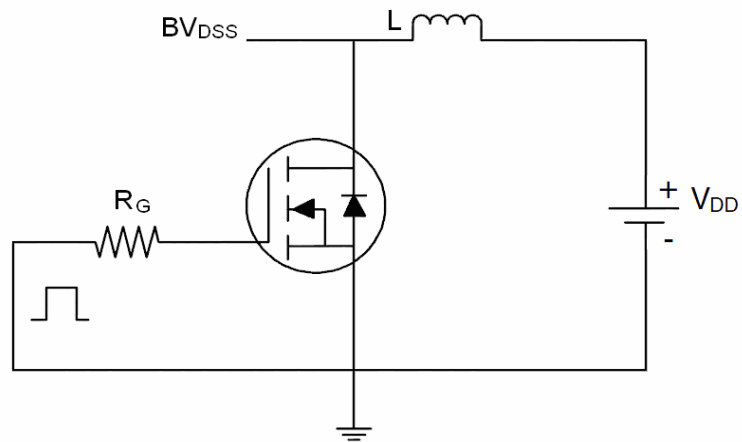
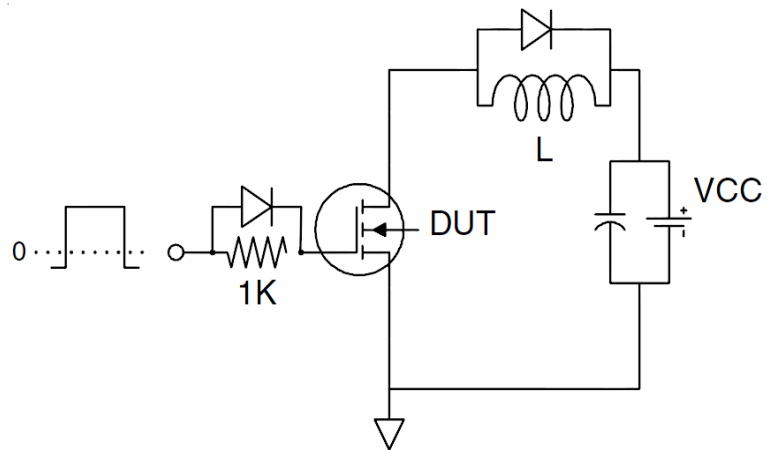
Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.68	°C/W
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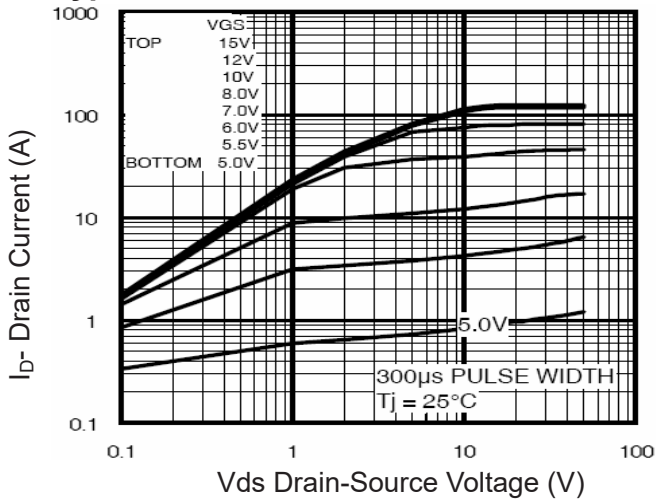
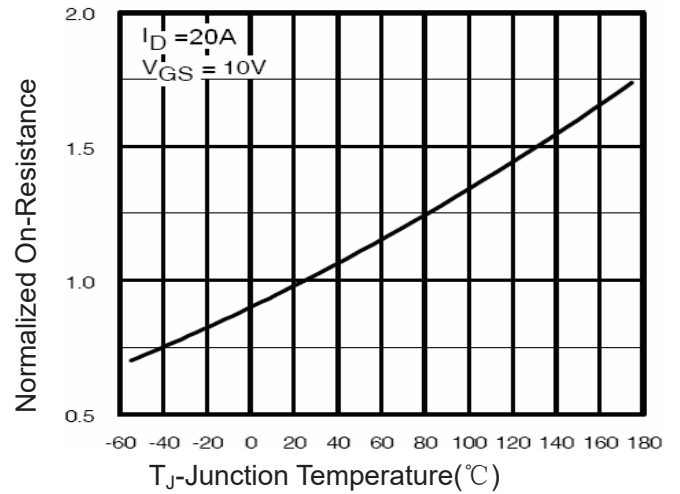
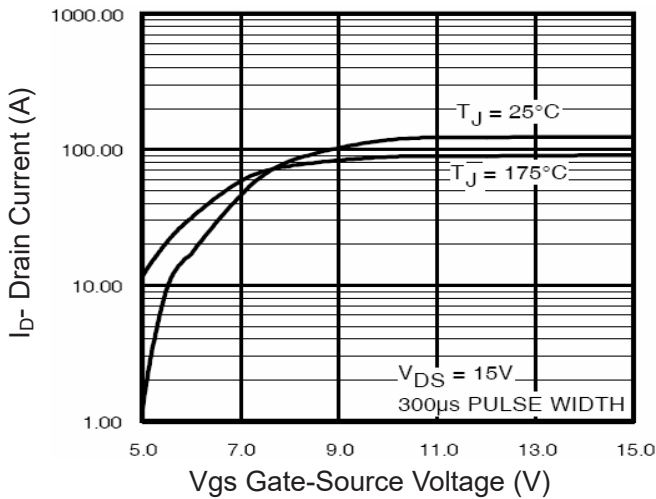
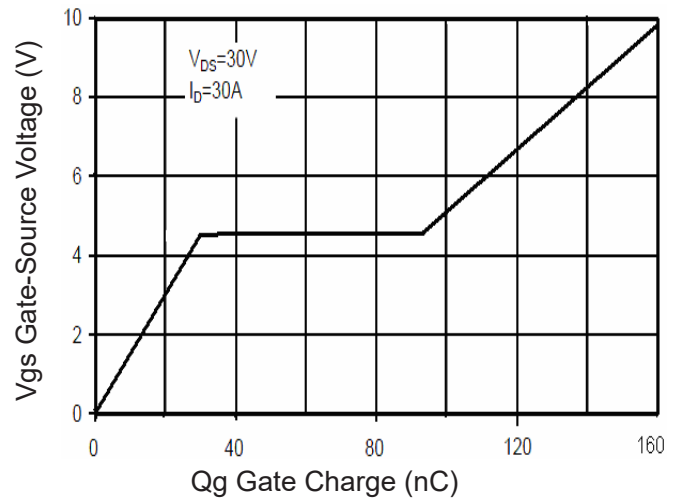
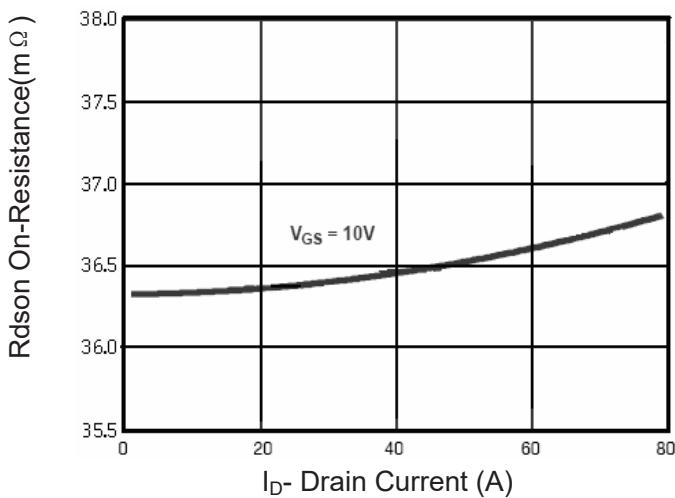
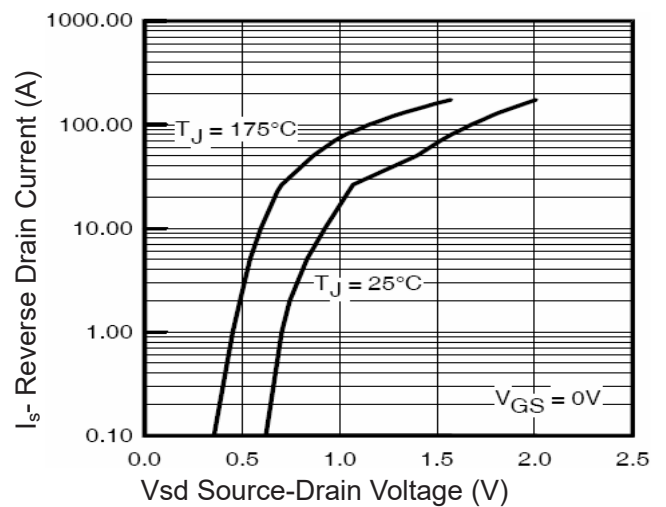
Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

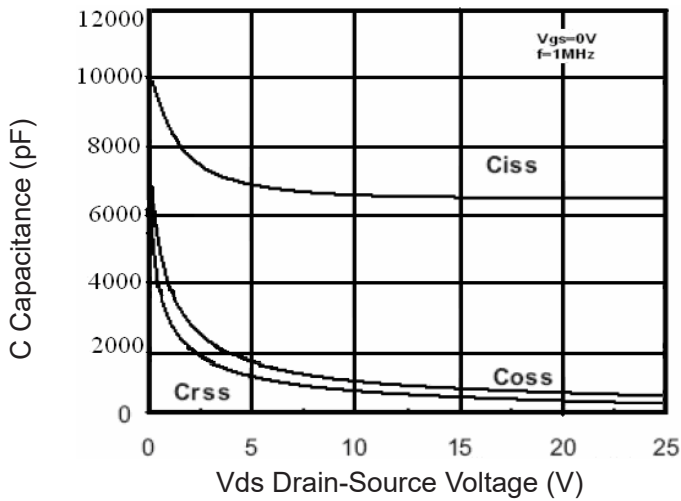
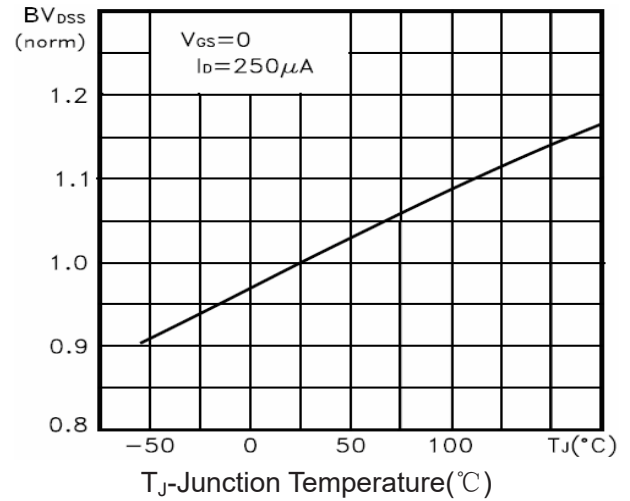
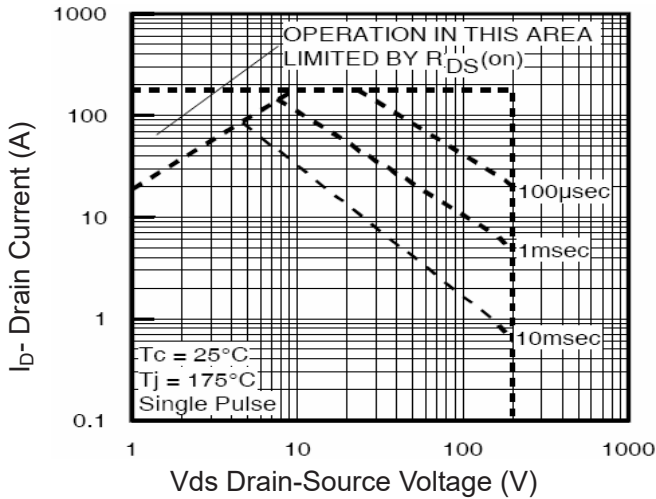
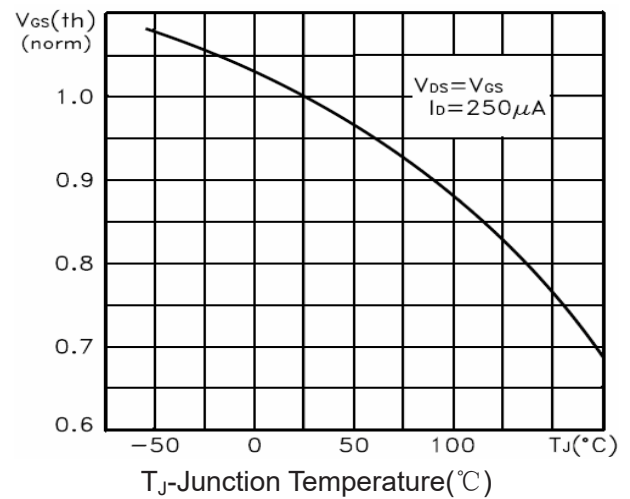
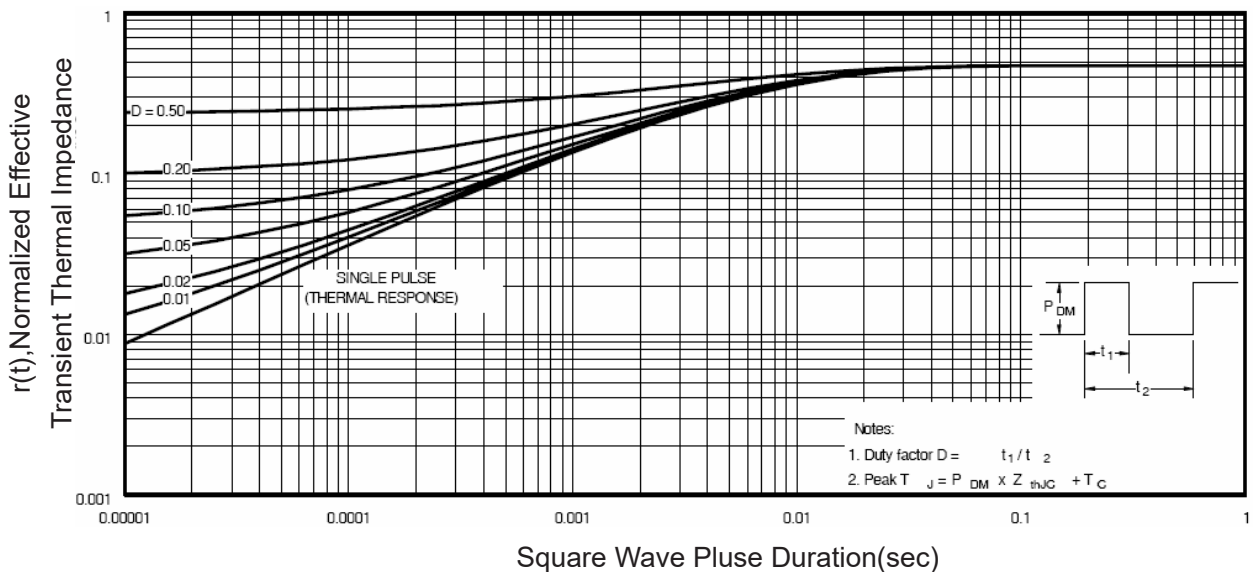
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	200	220	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=200V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3.2	4	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	36.4	41	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=25V, I_D=25A$	26	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	6500	-	PF
Output Capacitance	C_{oss}		-	290	-	PF
Reverse Transfer Capacitance	C_{rss}		-	220	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$	-	26	-	nS
Turn-on Rise Time	t_r		-	24	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	91	-	nS
Turn-Off Fall Time	t_f		-	39	-	nS
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=30A,$ $V_{GS}=10V$	-	163	-	nC
Gate-Source Charge	Q_{gs}		-	31	-	nC
Gate-Drain Charge	Q_{gd}		-	64	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=40A$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	40	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 40A$ $di/dt = 100A/\mu\text{s}$ ^(Note 3)	-	42	-	nS
Reverse Recovery Charge	Q_{rr}		-	66	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: $j=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Test Circuit
1) E_{AS} test Circuits

2) Gate charge test Circuit

3) Switch Time Test Circuit


Typical Electrical and Thermal Characteristics (Curves)

Figure 1 Output Characteristics

Figure 4 $R_{ds(on)}$ -Junction Temperature

Figure 2 Transfer Characteristics

Figure 5 Gate Charge

Figure 3 $R_{ds(on)}$ - Drain Current

Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 BV_{DSS} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 $V_{GS(th)}$ vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance