

Description

The VSM5N15 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

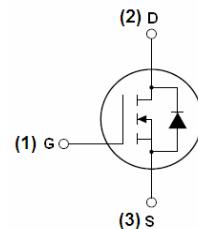
- $V_{DS} = 150V, I_D = 5.2A$
- $R_{DS(ON)} < 44m\Omega @ V_{GS}=10V$ (Typ: $31m\Omega$)
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Low gate to drain charge to reduce switching losses

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



SOP-8



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM5N15-S8	VSM5N15	SOP-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	5.2	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D (100^\circ C)$	3.7	A
Pulsed Drain Current(Note 1)	I_{DM}	42	A
Maximum Power Dissipation	P_D	3.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^{Note 2)}	$R_{\theta JA}$	35.7	°C/W
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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

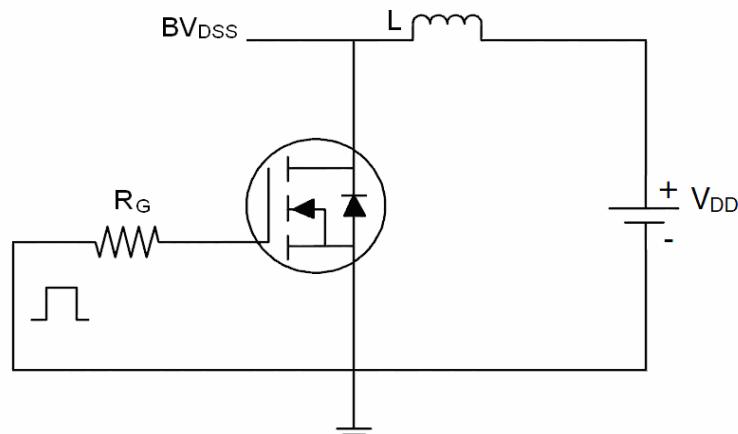
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=250\mu\text{A}$	150	170	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$\text{V}_{\text{DS}}=150\text{V}, \text{V}_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$\text{V}_{\text{GS}}=\pm 20\text{V}, \text{V}_{\text{DS}}=0\text{V}$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$\text{V}_{\text{GS}(\text{th})}$	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=250\mu\text{A}$	2.5	3.2	4.5	V
Drain-Source On-State Resistance	$\text{R}_{\text{DS}(\text{ON})}$	$\text{V}_{\text{GS}}=10\text{V}, \text{I}_D=5.2\text{A}$	-	31	44	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$\text{V}_{\text{DS}}=50\text{V}, \text{I}_D=5.2\text{A}$	12	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$\text{V}_{\text{DS}}=25\text{V}, \text{V}_{\text{GS}}=0\text{V},$ $F=1.0\text{MHz}$	-	1700	-	PF
Output Capacitance	C_{oss}		-	190	-	PF
Reverse Transfer Capacitance	C_{rss}		-	90	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$\text{V}_{\text{DD}}=75\text{V}, \text{I}_D=3.1\text{A}$ $\text{V}_{\text{GS}}=10\text{V}, \text{R}_{\text{GEN}}=6.5\Omega$	-	15	-	nS
Turn-on Rise Time	t_r		-	13	-	nS
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	26	-	nS
Turn-Off Fall Time	t_f		-	14	-	nS
Total Gate Charge	Q_g	$\text{V}_{\text{DS}}=75\text{V}, \text{I}_D=3.1\text{A},$ $\text{V}_{\text{GS}}=10\text{V}$	-	35.8	-	nC
Gate-Source Charge	Q_{gs}		-	7.5	-	nC
Gate-Drain Charge	Q_{gd}		-	13	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_S=3.1\text{A}$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	2.7	A
Reverse Recovery Time	trr	$\text{T}_J = 25^\circ\text{C}, \text{I}_F = 3.1\text{A},$ $d\text{i}/dt = 100\text{A}/\mu\text{s}$	-	50	-	nS
Reverse Recovery Charge	Qrr		-	140	-	nC

Notes:

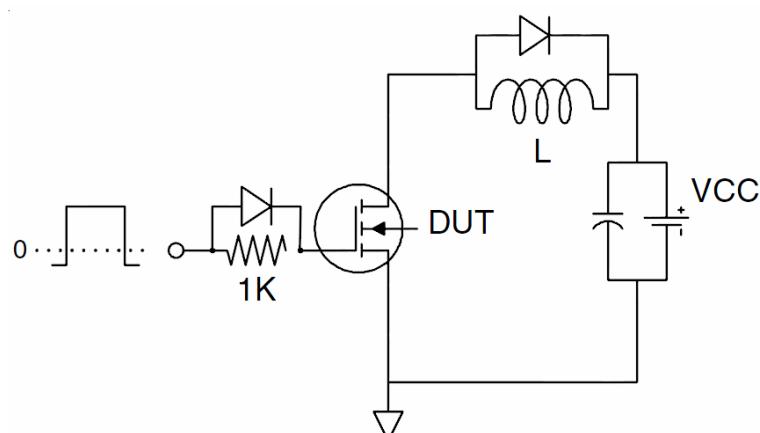
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production.

Test Circuit

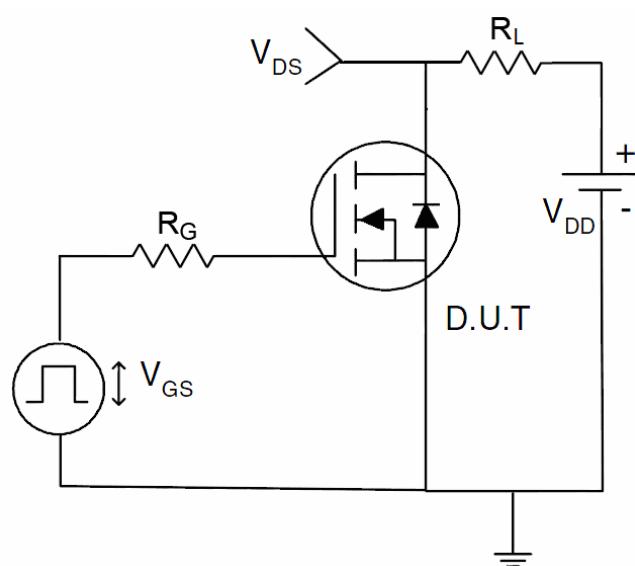
1) E_{AS} test Circuits



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

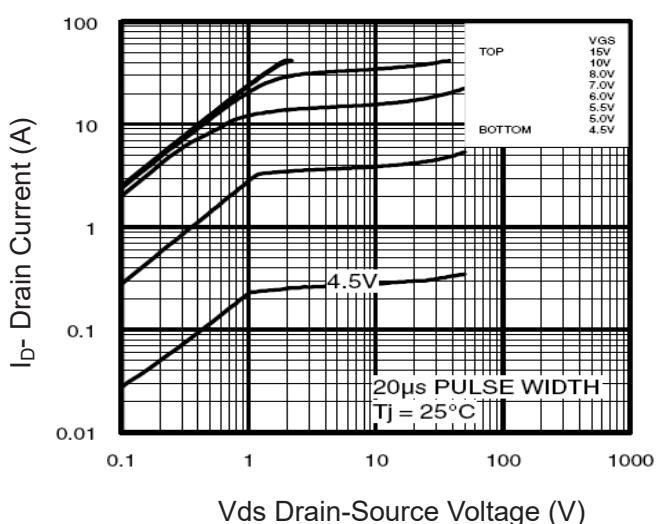


Figure 1 Output Characteristics

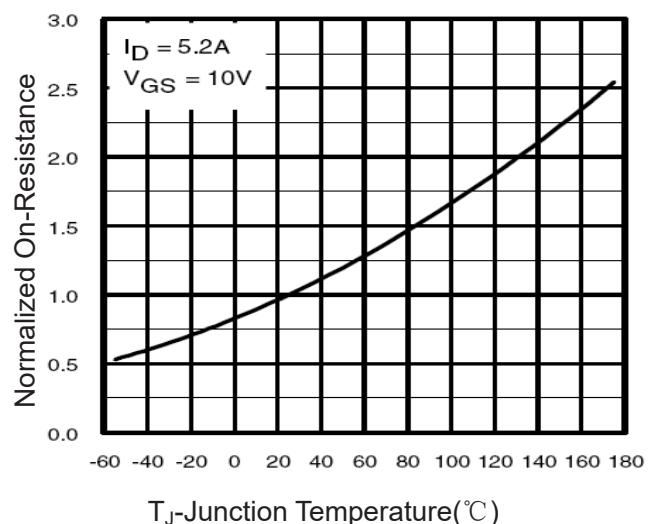


Figure 4 Rdson-JunctionTemperature

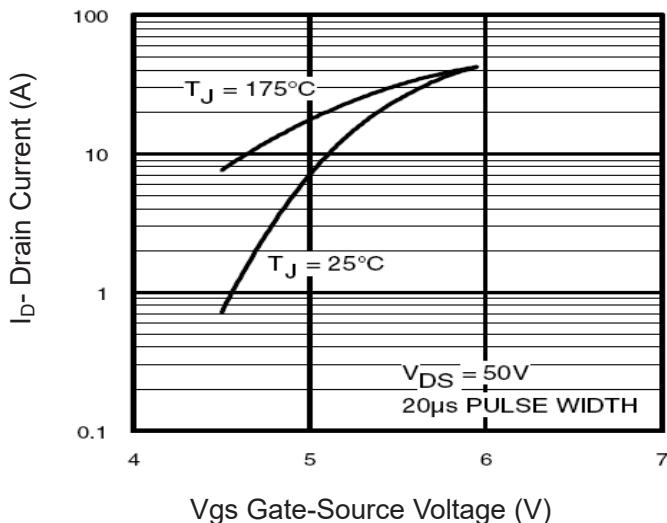


Figure 2 Transfer Characteristics

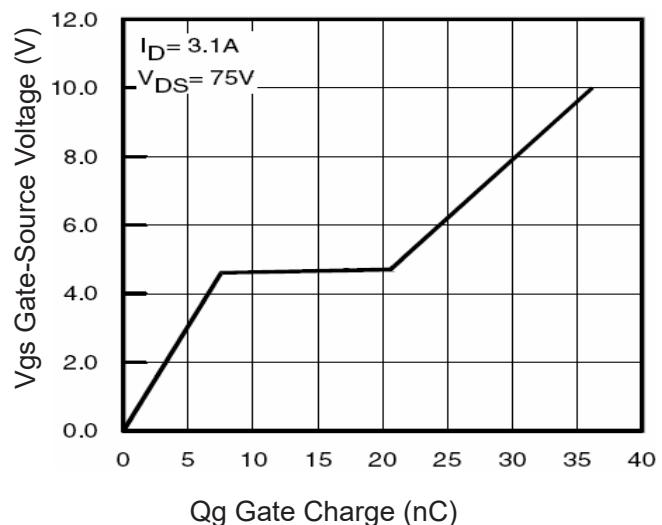


Figure 5 Gate Charge

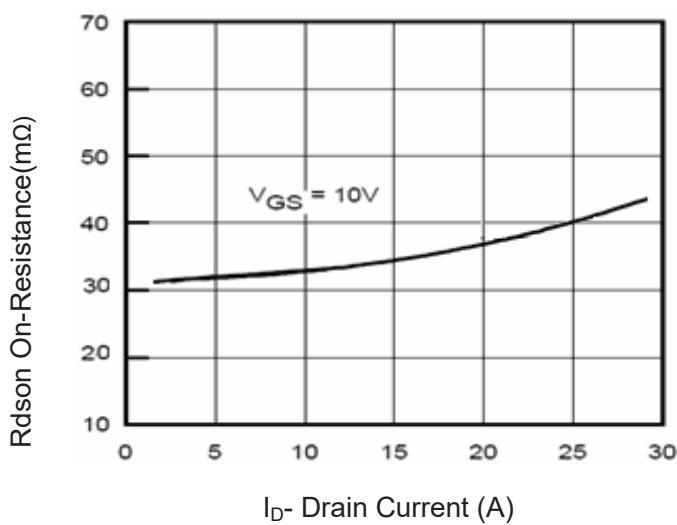


Figure 3 Rdson- Drain Current

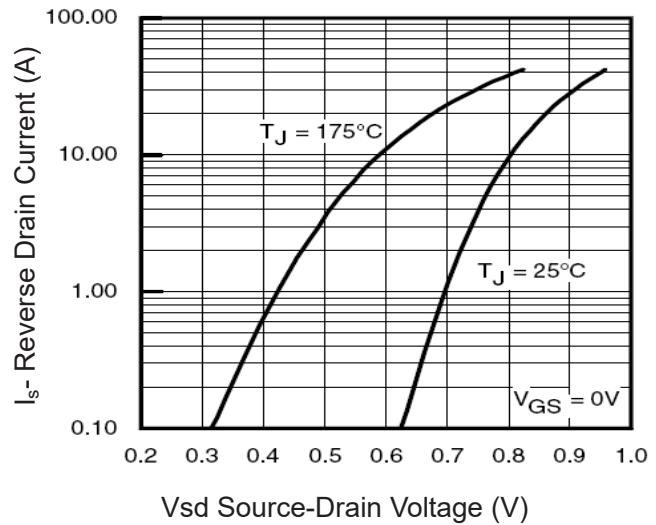
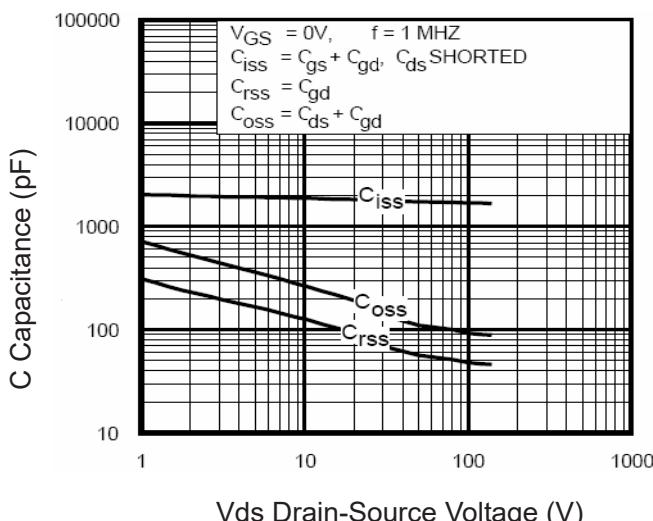
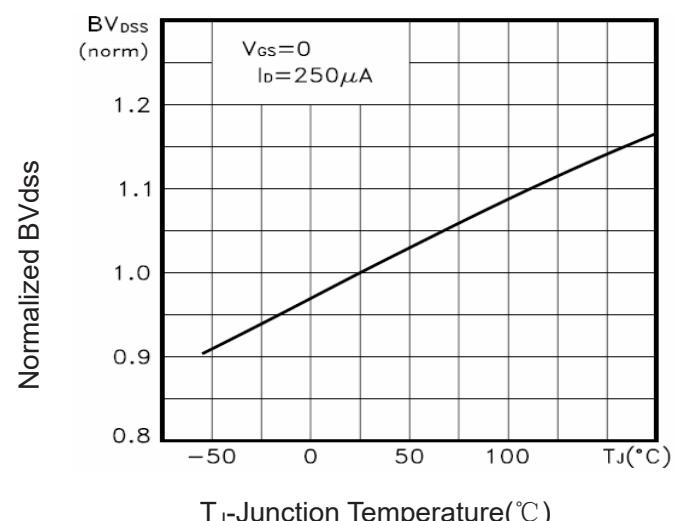
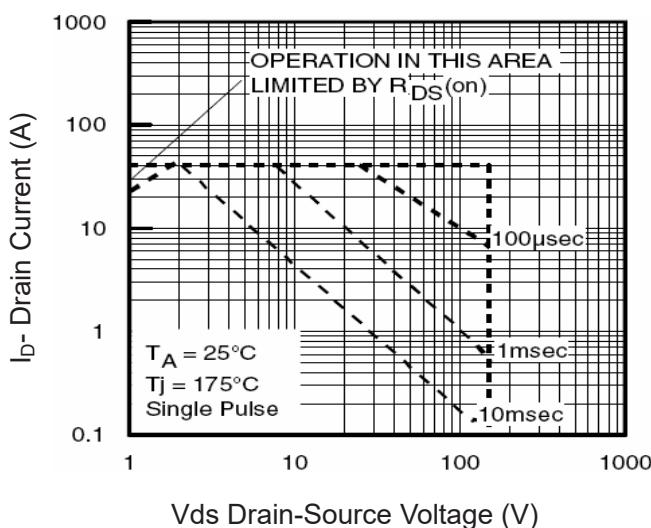
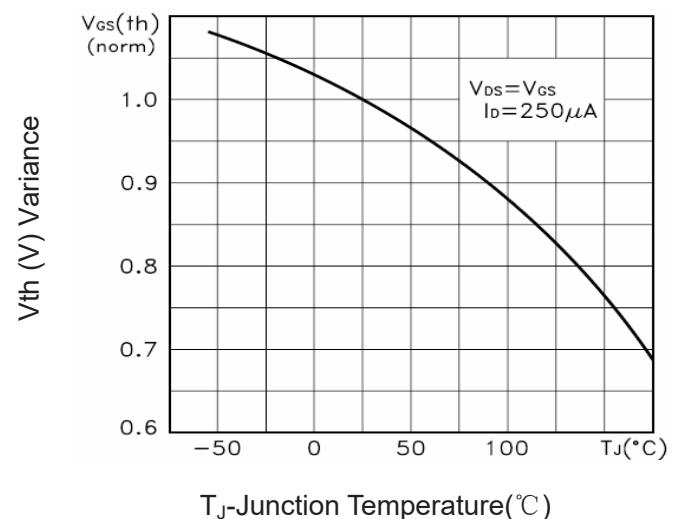
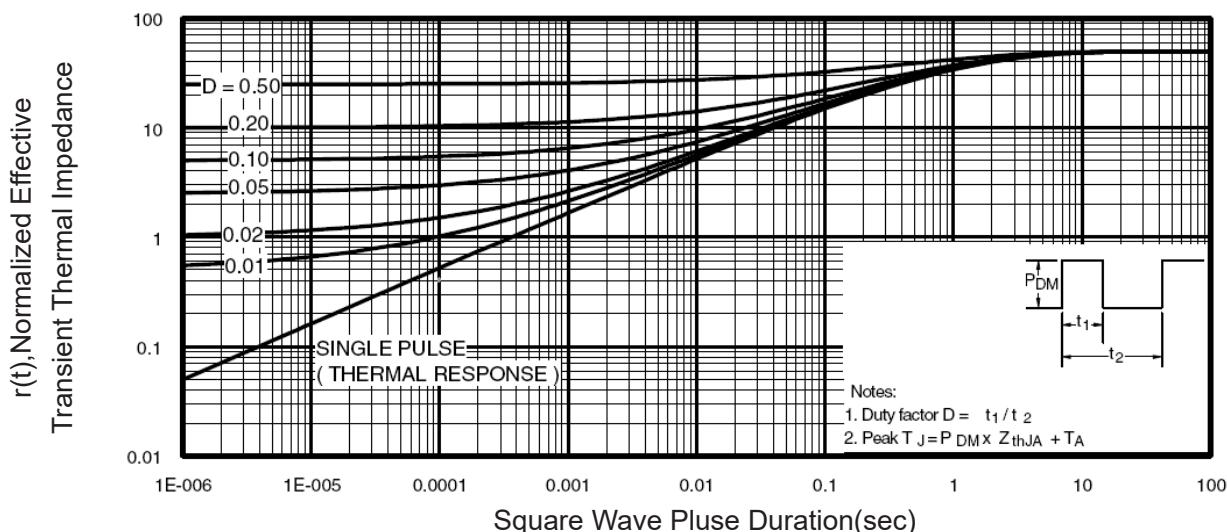


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 BV_{DSS} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 V_{GS(th)} vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance