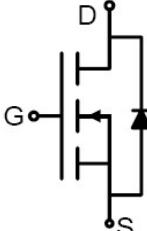


Description

Features <ul style="list-style-type: none"> ● 20V,75A $R_{DS(ON)} < 5m\Omega$ @ $V_{GS} = 4.5V$ $R_{DS(ON)} < 9m\Omega$ @ $V_{GS} = 2.5V$ ● Advanced Trench Technology ● Excellent $R_{DS(ON)}$ and Low Gate Charge ● Lead free product is acquired 	Application <ul style="list-style-type: none"> ● Load Switch ● PWM Application ● Power management <p>100% UIS 100% ΔV_{ds}</p>
 TO-252	 Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
VSM75N02-T2	VSM75N02	TAPING	TO-252	13inch	2500	25000

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		± 12	V
I_D	Continuous Drain Current		75	A
	$T_c = 100^\circ C$	49	A	
I_{DM}	Pulsed Drain Current ^{note1}		300	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		56.2	mJ
P_D	Power Dissipation	$T_c = 25^\circ C$	57	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		2.63	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	$^\circ C$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}$, $V_{GS}=0\text{V}$,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 12\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.4	0.7	1.1	V
$R_{DS(\text{on})}$ note3	Static Drain-Source on-Resistance	$V_{GS}=4.5\text{V}$, $I_D=30\text{A}$	-	4.1	5	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}$, $I_D=20\text{A}$	-	6.5	9	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=10\text{V}$, $V_{GS}=0\text{V}$, $f = 1.0\text{MHz}$	-	2500	-	pF
C_{oss}	Output Capacitance		-	407	-	pF
C_{rss}	Reverse Transfer Capacitance		-	386	-	pF
Q_g	Total Gate Charge	$V_{DS}=10\text{V}$, $I_D=30\text{A}$, $V_{GS}=4.5\text{V}$	-	32	-	nC
Q_{gs}	Gate-Source Charge		-	3	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	11	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=10\text{V}$, $I_D=30\text{A}$, $R_{\text{GEN}}=3\Omega$, $V_{GS} = 4.5\text{V}$	-	17	-	ns
t_r	Turn-on Rise Time		-	49	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	74	-	ns
t_f	Turn-off Fall Time		-	26	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	75	A	
I_{sM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	300	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}$, $I_s=30\text{A}$	-	-	1.2	V

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^\circ\text{C}$, $V_{DD}=10\text{V}$, $V_G=4.5\text{V}$, $L=0.5\text{mH}$, $R_G=25\Omega$, $I_{AS}=15\text{A}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical Performance Characteristics

Figure1: Output Characteristics

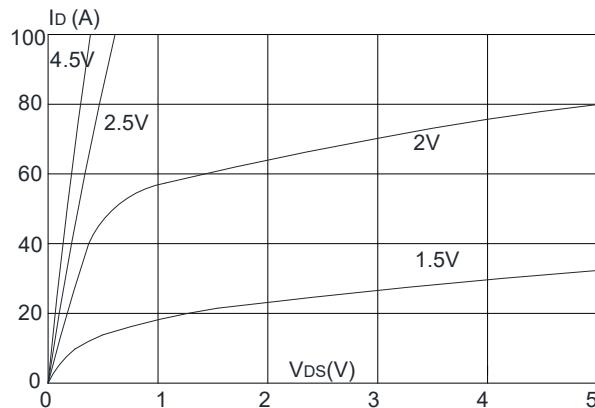


Figure 3: On-resistance vs. Drain Current

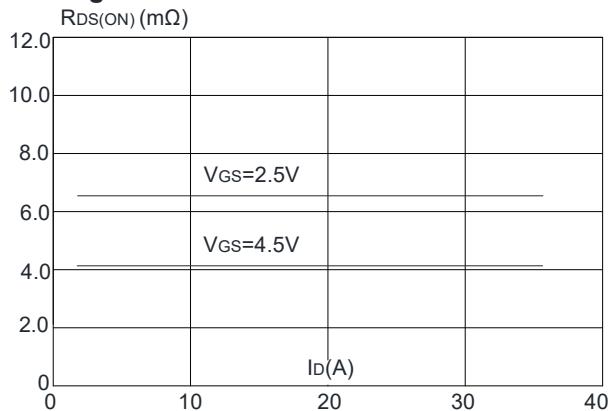


Figure 5: Gate Charge Characteristics

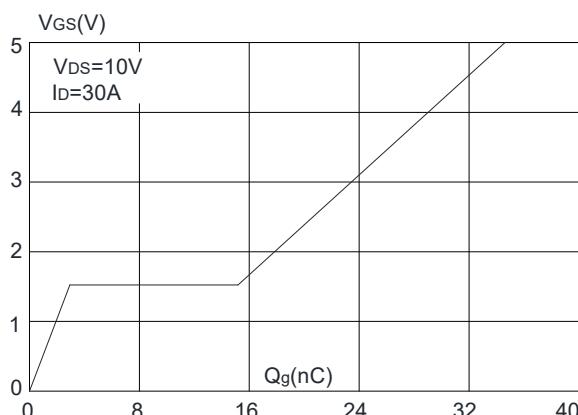


Figure 2: Typical Transfer Characteristics

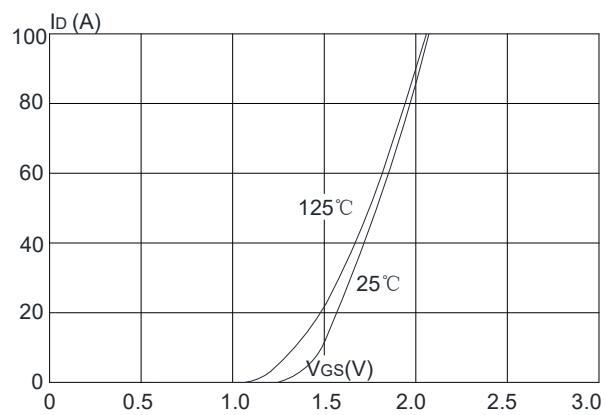


Figure 4: Body Diode Characteristics

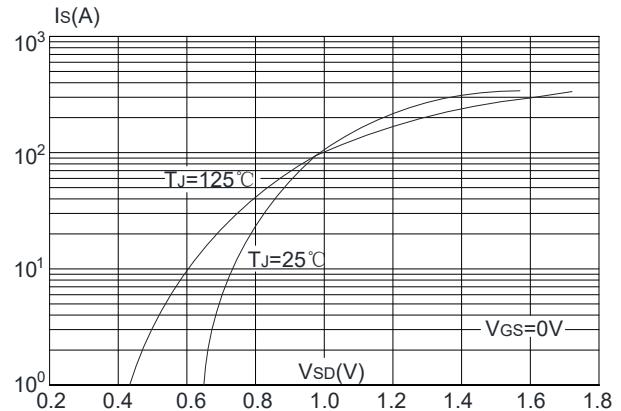


Figure 6: Capacitance Characteristics

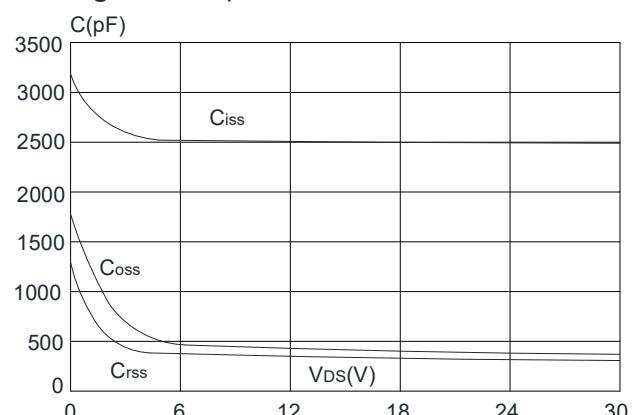


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

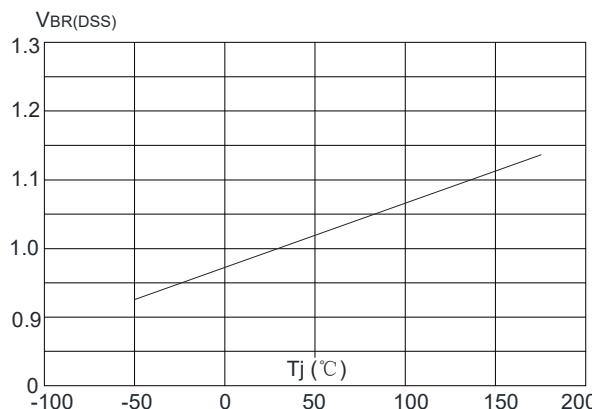


Figure 9: Maximum Safe Operating Area

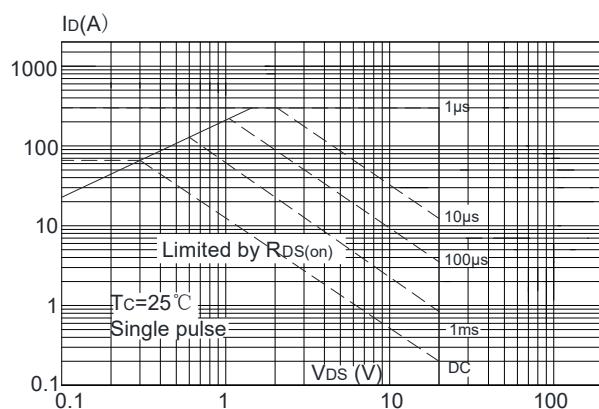


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

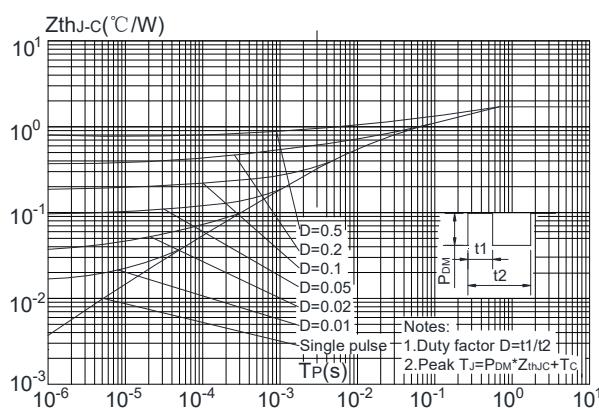


Figure 8: Normalized on Resistance vs. Junction Temperature

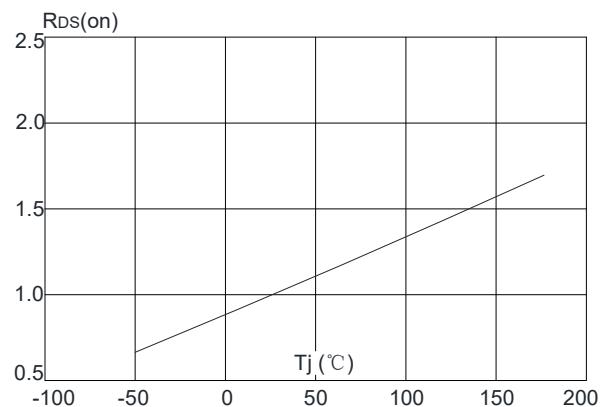
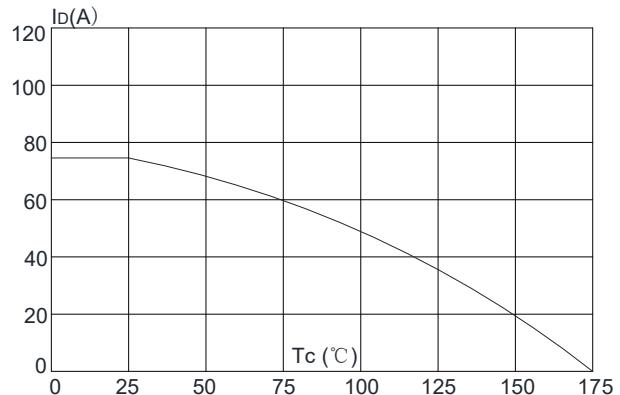


Figure 10: Maximum Continuous Drain Current vs. Case Temperature



Test Circuit

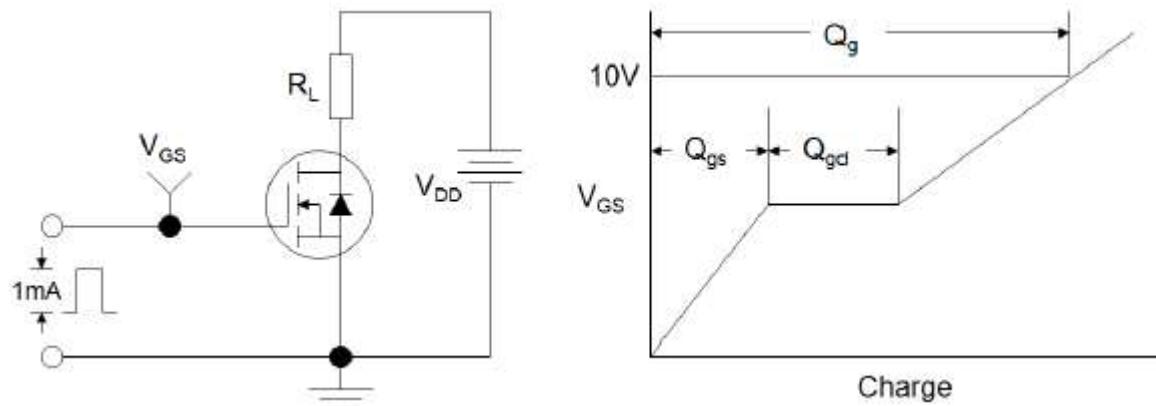


Figure1:Gate Charge Test Circuit & Waveform

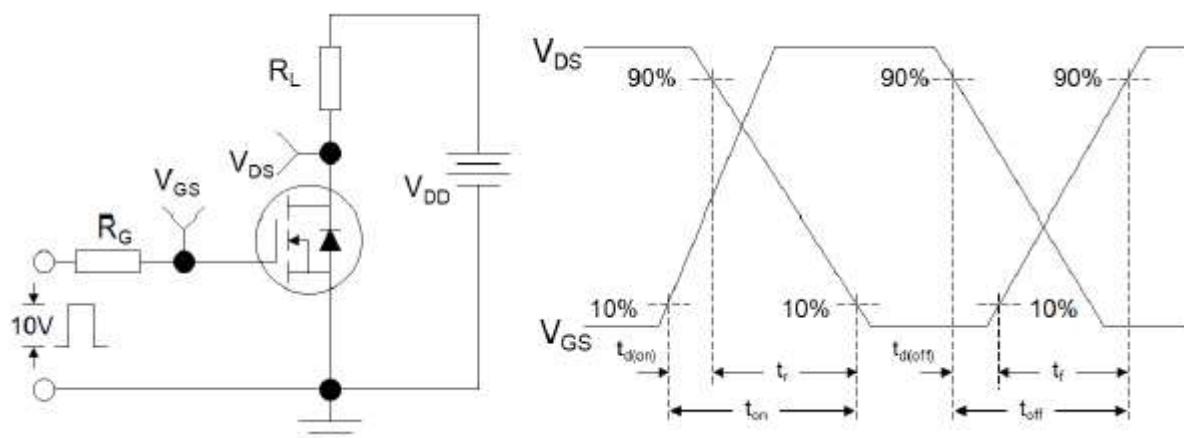


Figure 2: Resistive Switching Test Circuit & Waveforms

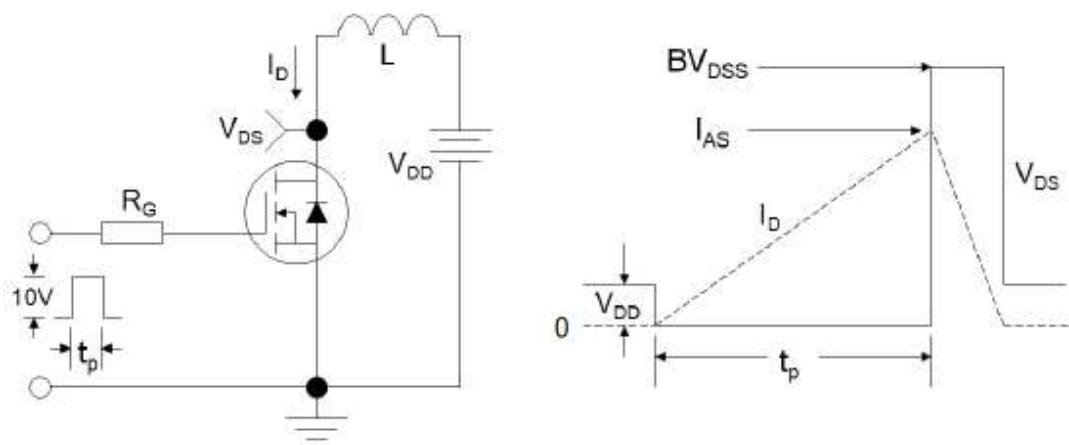


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms