

Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

- ◆ 100V, 80A, $R_{DS(on),max}=18m\Omega @ V_{GS}=10V$
- ◆ Improved dv/dt capability
- ◆ Fast switching
- ◆ 100% EAS Guaranteed
- ◆ Green device available

Applications

- ◆ Motor Drives
- ◆ UPS
- ◆ DC-DC Converter

Product Summary

V_{DSS}	100V
$R_{DS(on),max} @ V_{GS}=10V$	18mΩ
I_D	80A

Pin Configuration



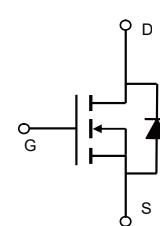
TO-263



TO-220C



TO-220F



Schematic

Absolute Maximum Ratings

 $T_c = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	V
Continuous drain current ($T_c = 25^\circ C$) ¹⁾	I_D	80	A
Continuous drain current ($T_c = 100^\circ C$) ¹⁾		57	A
Pulsed drain current ²⁾	I_{DM}	320	A
Gate-Source voltage	V_{GSS}	± 20	V
Avalanche energy ³⁾	E_{AS}	240	mJ
Power Dissipation ($T_c = 25^\circ C$ C C TO-220/TO-263)	P_D	147	W
Power Dissipation ($T_c = 25^\circ C$ C C TO-220F)		49	W
Storage Temperature Range	T_{STG}	-55 to +150	°C
Operating Junction Temperature Range	T_J	-55 to +150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case C C TO-220/TO-263	$R_{\theta JC}$	0.85	°C/W
Thermal Resistance, Junction-to-Case C C TO-220F		2.55	°C/W
Thermal Resistance, Junction-to-Ambient C C TO-220/TO-263	$R_{\theta JA}$	62	°C/W
Thermal Resistance, Junction-to-Ambient C C TO-220F		80	°C/W

Package Marking and Ordering Information

Device	Device Package	Marking
VSM80N10-T3	TO-263	VSM80N10-T3
VSM80N10-TF	TO-220F	VSM80N10-TF
VSM80N10-TC	TO-220C	VSM80N10-TC

Electrical Characteristics

T_J = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0 V, I _D =250μA	100	---	---	V
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	---	3.0	V
Drain-source leakage current	I _{DSS}	V _{DS} =100V, V _{GS} =0V, T _J = 25°C	---	---	1	μA
		V _{DS} =80V, V _{GS} =0V, T _J = 125°C	---	---	10	μA
Gate leakage current, Forward	I _{GSSF}	V _{GS} =20 V, V _{DS} =0 V	---	---	100	nA
Gate leakage current, Reverse	I _{GSSR}	V _{GS} =-20 V, V _{DS} =0 V	---	---	-100	nA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =10 V, I _D =16 A	---	13.5	18	mΩ
		V _{GS} =4.5 V, I _D =8 A	---	16	23	mΩ
Forward transconductance	g _{fs}	V _{DS} =10V , I _D =20A	---	85	---	S
Dynamic characteristics						
Input capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, F = 1MHz	---	6102	---	pF
Output capacitance	C _{oss}		---	215	---	
Reverse transfer capacitance	C _{rss}		---	159	---	
Turn-on delay time	t _{d(on)}	V _{DD} = 50V, V _{GS} =10V, I _D = 20A	---	20	---	ns
Rise time	t _r		---	56	---	
Turn-off delay time	t _{d(off)}		---	75	---	
Fall time	t _f		---	36	---	
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, F=1MHz	---	1.5	---	Ω
Gate charge characteristics						
Gate to source charge	Q _{gs}	V _{DS} =50 V, I _D =20A, V _{GS} = 10 V	---	18	---	nC
Gate to drain charge	Q _{gd}		---	32	---	
Gate charge tota	Q _g		---	127	---	
Drain-Source diode characteristics and Maximum Ratings						
Diode Forward Voltage ⁴⁾	V _{SD}	V _{GS} =0V, I _S =50A, T _J =25°C	---	0.85	1.3	V
Reverse Recovery Time	t _{rr}	I _S =20A, di/dt=60A/us, T _J =25°C	---	160	---	ns
Reverse Recovery Charge	Q _{rr}		---	136	---	nC

Notes:

- 1: The maximum junction current rating is package limited.
- 2: Repetitive Rating: Pulse width limited by maximum junction temperature.
- 3: V_{DD}=50V, V_{GS}=10V, L=0.5mH, I_{AS}=31A, R_G=25Ω, Starting T_J=25°C.
- 4: Pulse Test: Pulse Width ≤300 μ s, Duty Cycle≤2%.

Electrical Characteristics Diagrams

Figure 1. Typ. Output Characteristics

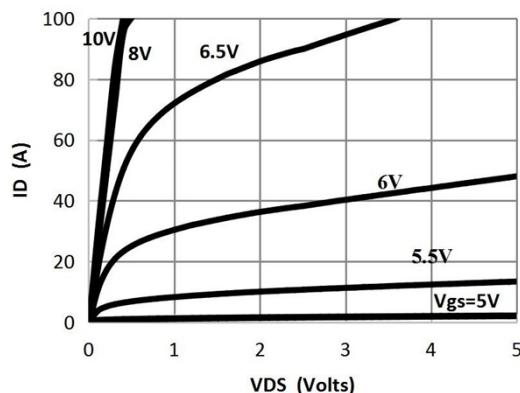


Figure 2. Transfer Characteristics

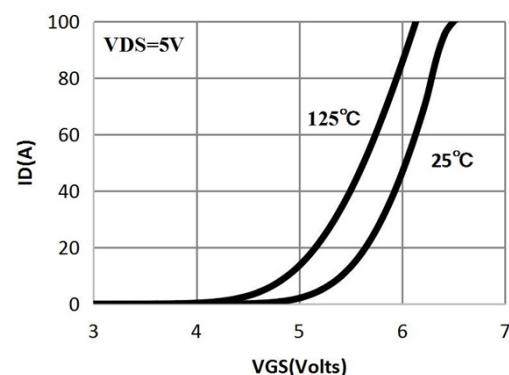


Figure 3. Capacitance Characteristics

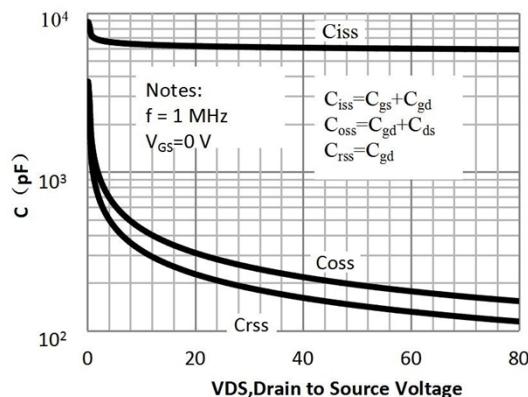


Figure 4. Gate Charge Waveform

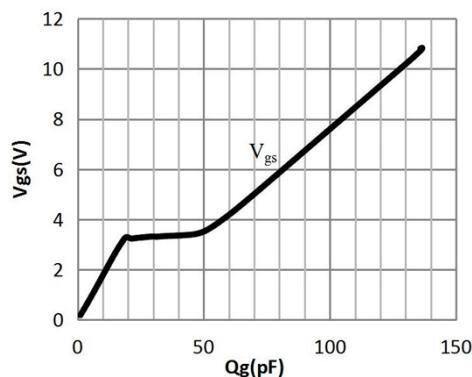


Figure 5. Body-Diode Characteristics

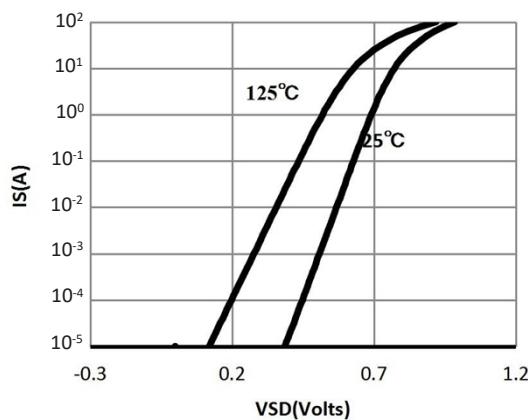


Figure 6. Maximum Safe Operating Area

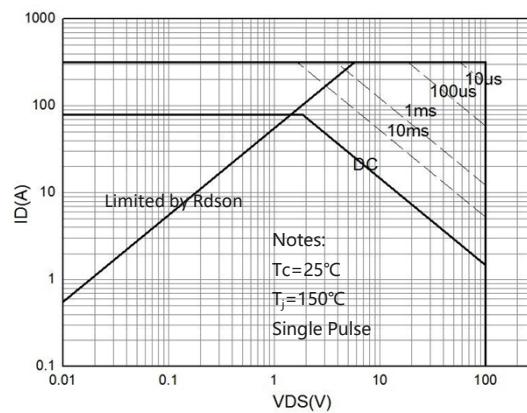


Figure 6. Normalized Maximum Transient Thermal Impedance (RthJC)

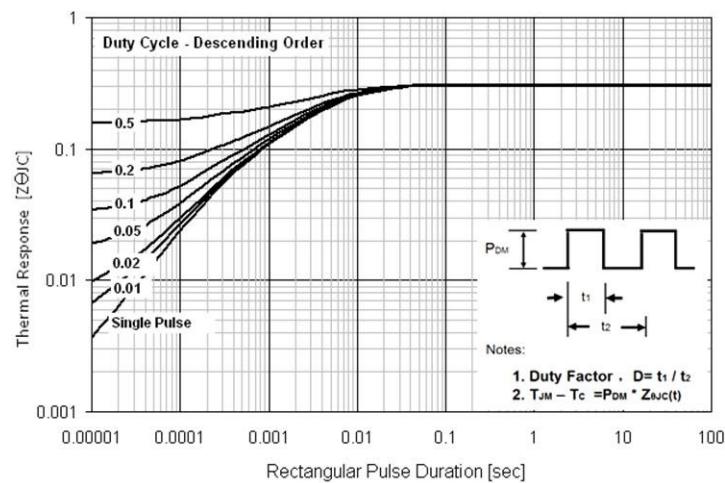
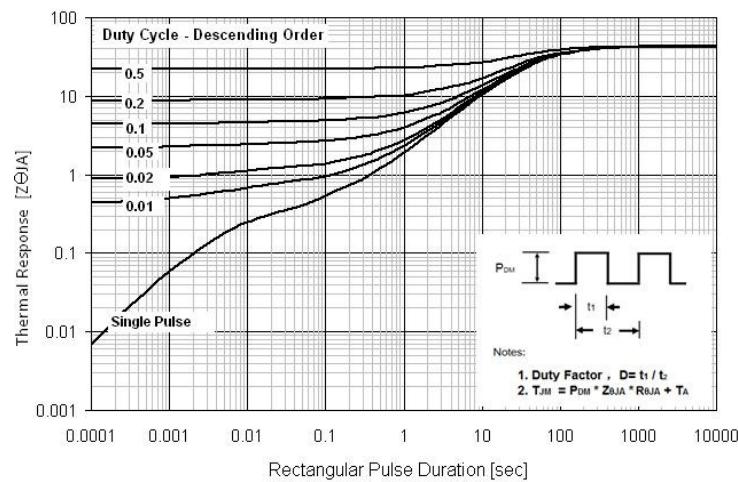


Figure 7. Normalized Maximum Transient Thermal Impedance (RthJA)



Test Circuit & Waveform

Figure 8. Gate Charge Test Circuit & Waveform

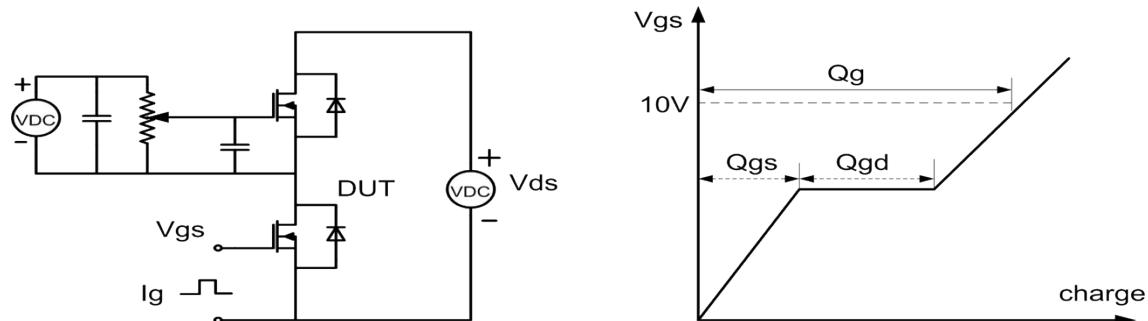


Figure 9. Resistive Switching Test Circuit & Waveforms

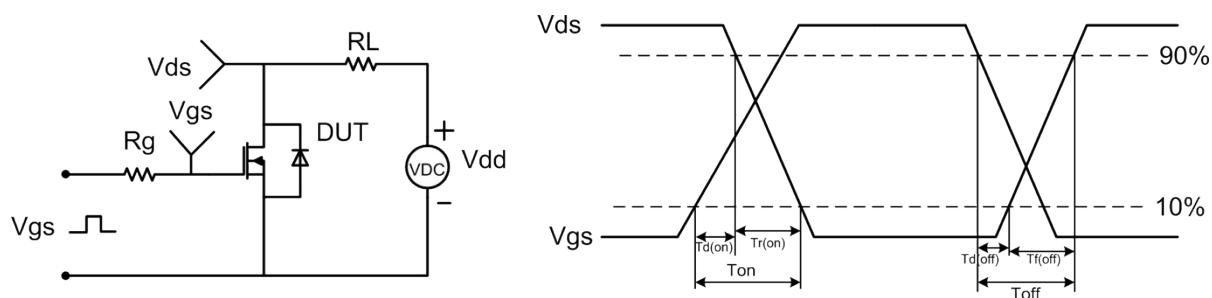


Figure 10. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

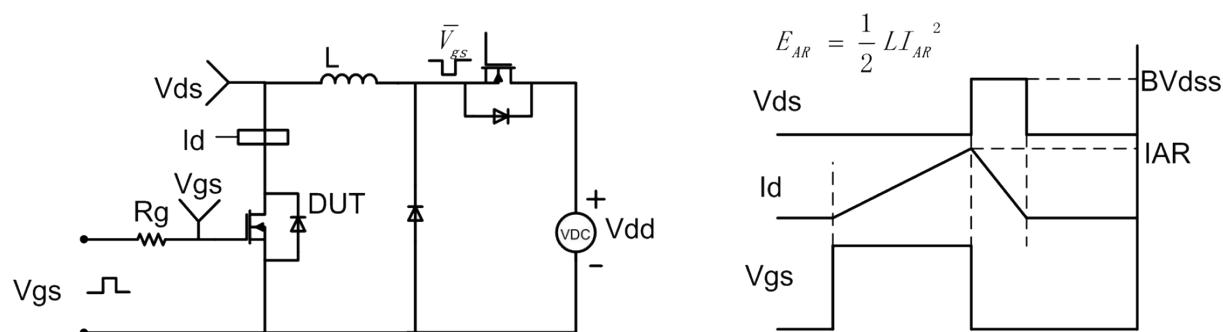


Figure 11. Diode Recovery Circuit & Waveform

