## Description

The VSM9N06 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

## General Features

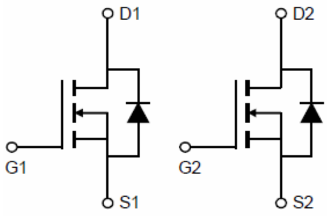
- $V_{DS}$ = 60V,$I_D$ =9A
  $R_{DS(ON)}$ < 15mΩ @ $V_{GS}$=10V (Typ:10mΩ)
  $R_{DS(ON)}$ < 18mΩ @ $V_{GS}$=4.5V (Typ:14mΩ)

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Low gate to drain charge to reduce switching losses

## Application

- Power switching application
- Load switch

SOP-8



Schematic Diagram

## Package Marking and Ordering Information

| Device Marking | Device | Device Package | Reel Size | Tape width | Quantity |
|---|---|---|---|---|---|
| VSM9N06-S8 | VSM9N06 | SOP-8 | - | - | - |

## Absolute Maximum Ratings ($T_C$=25℃unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 60 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Drain Current-Continuous | $I_D$ | 9 | A |
| Drain Current-Continuous($T_C$=100℃) | $I_D$ (100℃) | 6.4 | A |
| Pulsed Drain Current | $I_{DM}$ | 36 | A |
| Maximum Power Dissipation | $P_D$ | 2.6 | W |
| Operating Junction and Storage Temperature Range | $T_J$,$T_{STG}$ | -55 To 150 | ℃ |

## Thermal Characteristic

| | | | |
|---|---|---|---|
| Thermal Resistance,Junction-to-Ambient (Note 2) | $R_{\theta JA}$ | 48 | ℃/W |

## Electrical Characteristics (TC=25℃unless otherwise noted)

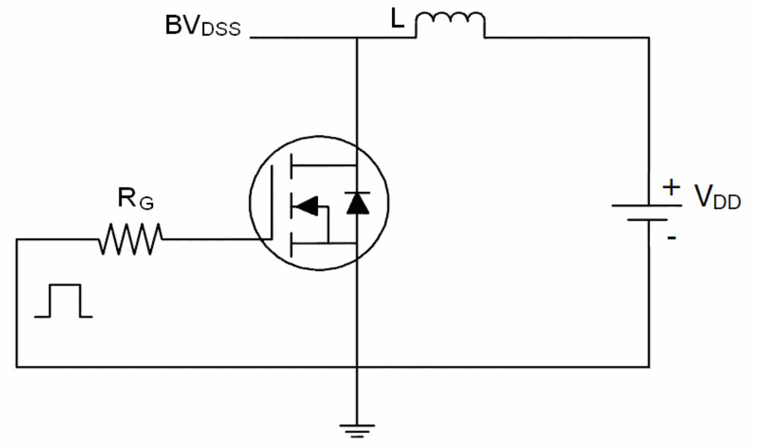
| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V $I_D$=250μA | 60 | | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=60V,$V_{GS}$=0V | - | - | 1 | μA |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V,$V_{DS}$=0V | - | - | ±100 | nA |
| **On Characteristics** (Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,$I_D$=250μA | 1.2 | 1.8 | 2.2 | V |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=9A | - | 10 | 15 | mΩ |
| | | $V_{GS}$=4.5V, $I_D$=9A | | 14 | 18 | mΩ |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$=5V,$I_D$=9A | 25 | - | - | S |
| **Dynamic Characteristics** (Note4) | | | | | | |
| Input Capacitance | $C_{lss}$ | $V_{DS}$=30V,$V_{GS}$=0V,<br>F=1.0MHz | - | 2180 | - | PF |
| Output Capacitance | $C_{oss}$ | | - | 350 | - | PF |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 270 | - | PF |
| **Switching Characteristics** (Note 4) | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$=30V, $R_L$=1Ω<br>$V_{GS}$=10V,$R_{GEN}$=3Ω | - | 8.5 | - | nS |
| Turn-on Rise Time | $t_r$ | | - | 6 | - | nS |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 30 | - | nS |
| Turn-Off Fall Time | $t_f$ | | - | 5 | - | nS |
| Total Gate Charge | $Q_g$ | $V_{DS}$=30V,$I_D$=9A,<br>$V_{GS}$=10V | - | 58 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 8 | - | nC |
| Gate-Drain Charge | $Q_{gd}$ | | - | 17 | - | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| Diode Forward Voltage (Note 3) | $V_{SD}$ | $V_{GS}$=0V,$I_S$=9A | - | - | 1.2 | V |
| Diode Forward Current (Note 2) | $I_S$ | - | - | - | 9 | A |
| Reverse Recovery Time | $t_{rr}$ | TJ = 25°C, IF=9A<br>di/dt = 100A/μs (Note3) | - | 30 | - | nS |
| Reverse Recovery Charge | Qrr | | - | 44 | - | nC |

## Notes:

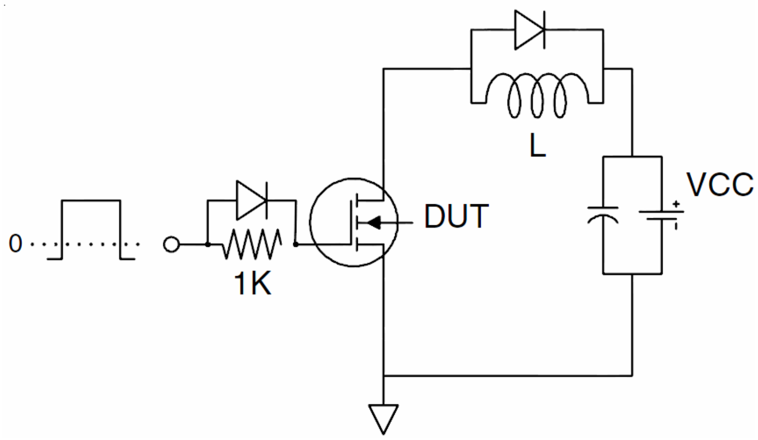
**1.** Repetitive Rating: Pulse width limited by maximum junction temperature.
**2.** Surface Mounted on FR4 Board, t ≤ 10 sec.
**3.** Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
**4.** Guaranteed by design, not subject to production
**5.** EAS condition：Tj=25℃,$V_{DD}$=50V,$V_G$=10V,L=0.5mH,Rg=25Ω

## Test Circuit

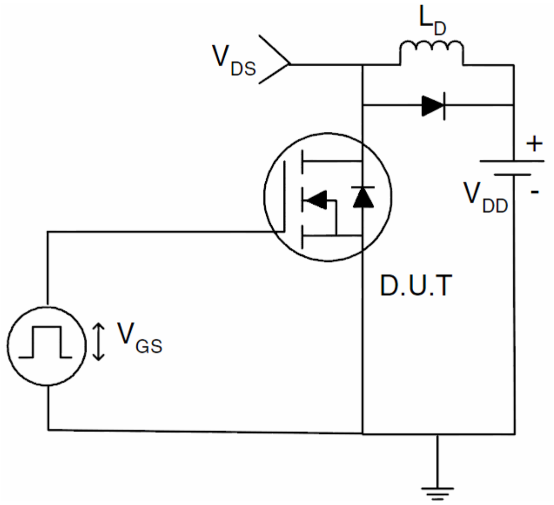
### 1) $E_{AS}$ test Circuit



### 2) Gate charge test Circuit



### 3) Switch Time Test Circuit



## Typical Electrical and Thermal Characteristics (Curves)

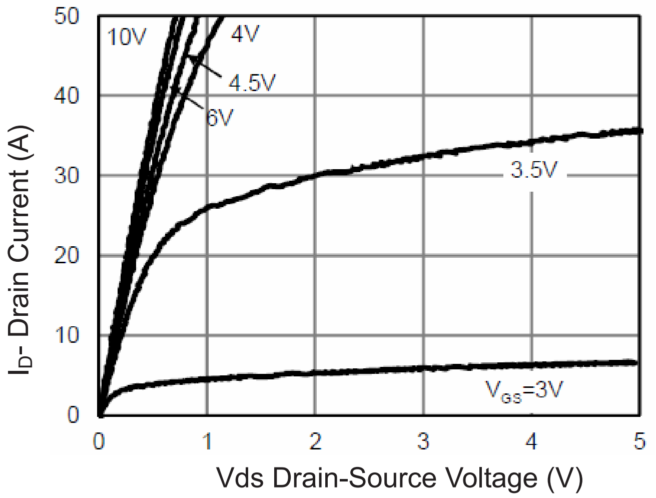


**Figure 1 Output Characteristics**

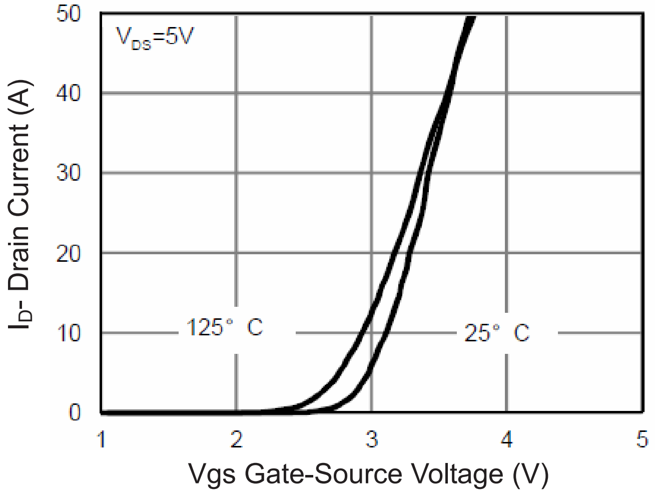


**Figure 2 Transfer Characteristics**

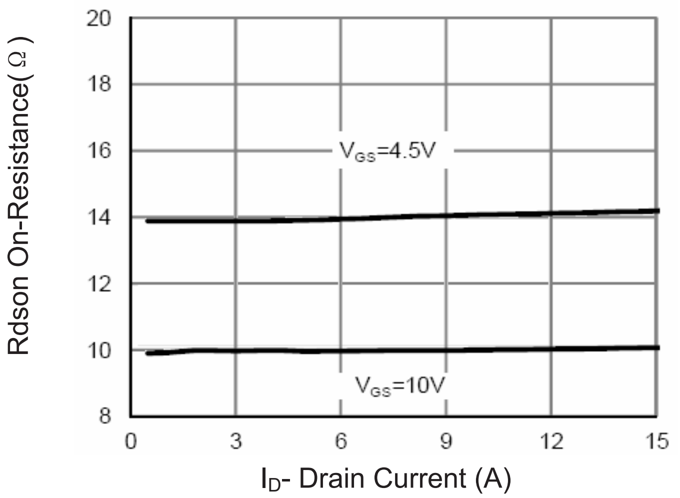


**Figure 3 Rdson- Drain Current**

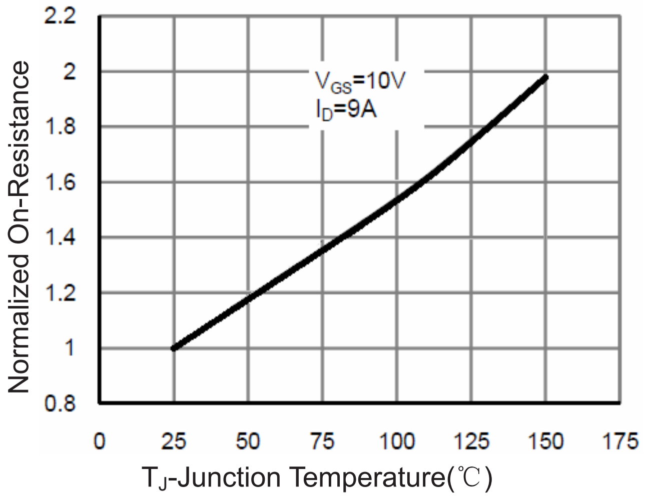


**Figure 4 Rdson-JunctionTemperature**

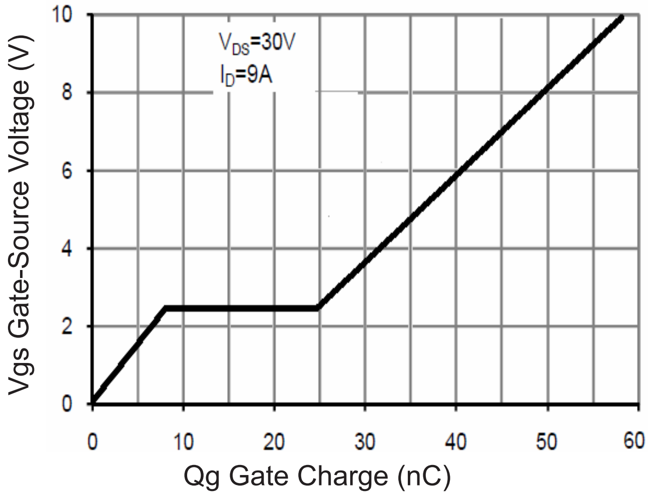


**Figure 5 Gate Charge**

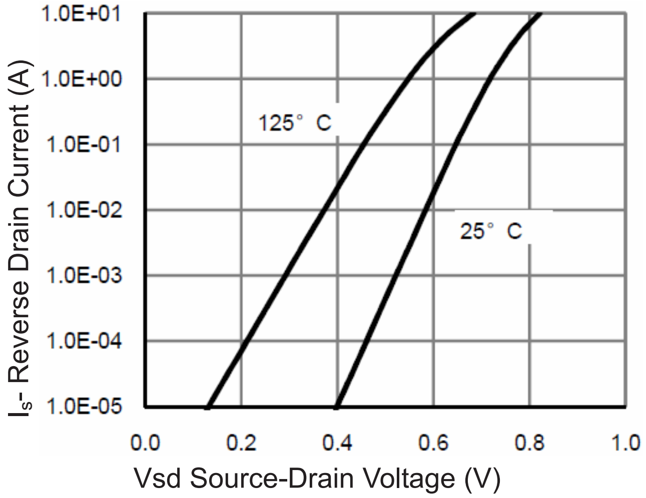


**Figure 6 Source- Drain Diode Forward**

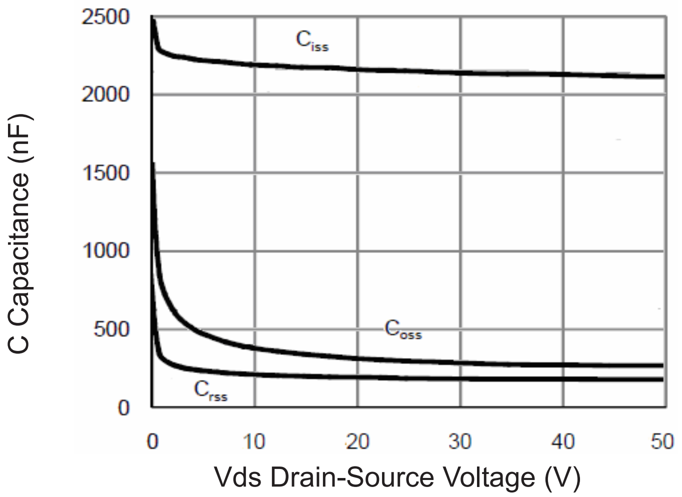


Figure 7 Capacitance vs Vds

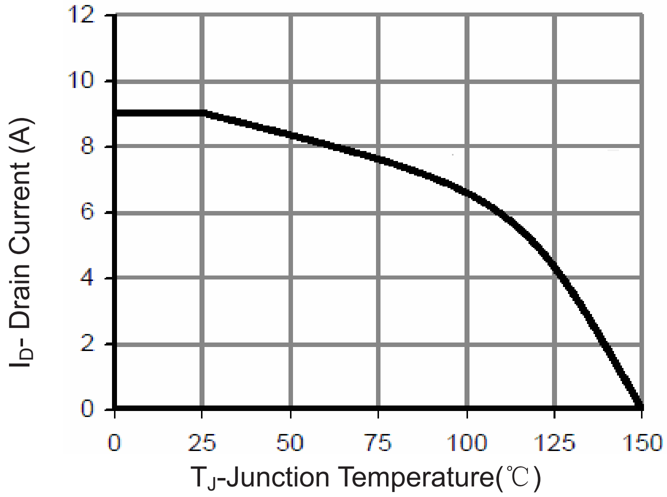


Figure 9 Current De-rating

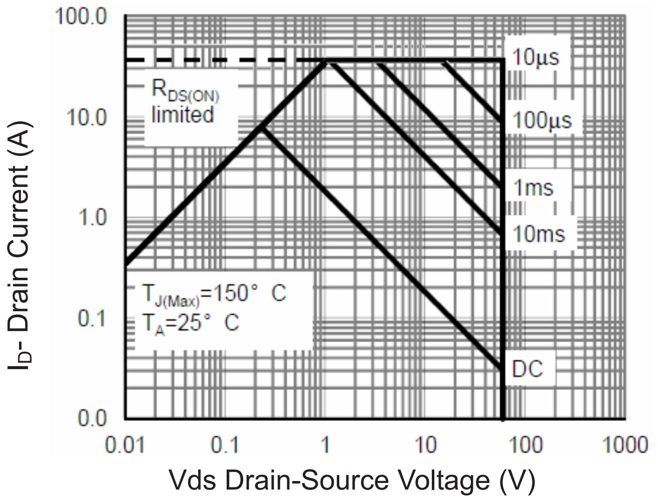


Figure 8 Safe Operation Area

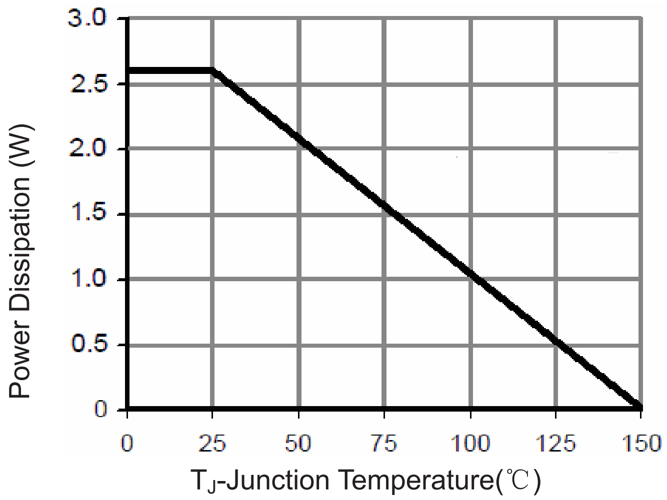


Figure 10 Power De-rating

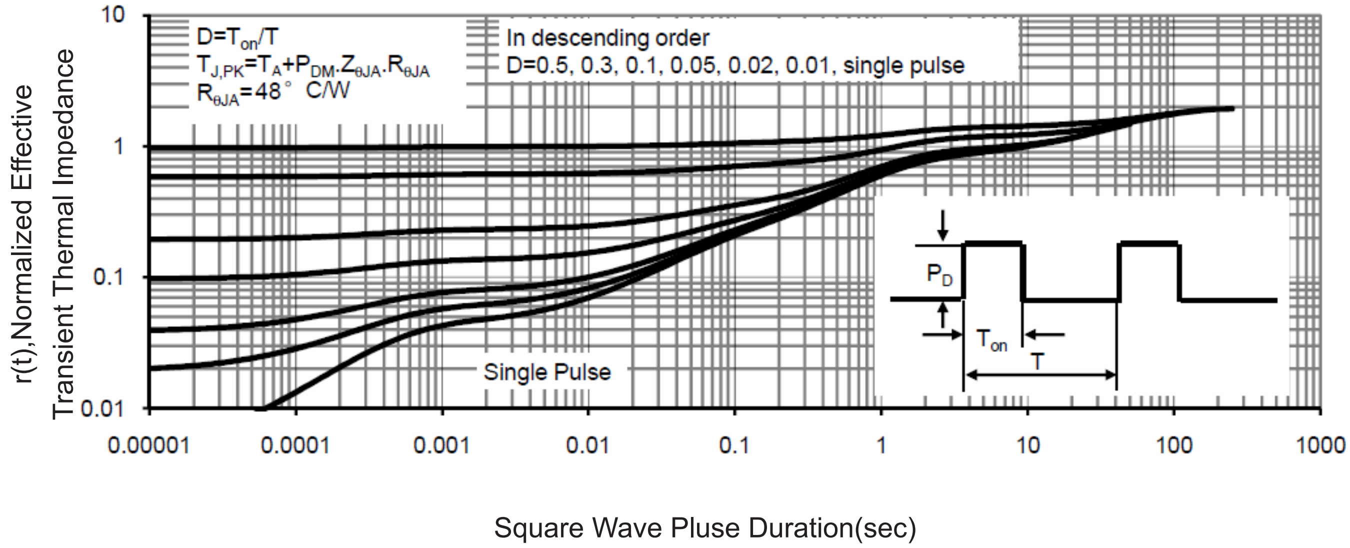


Figure 11 Normalized Maximum Transient Thermal Impedance