

Description

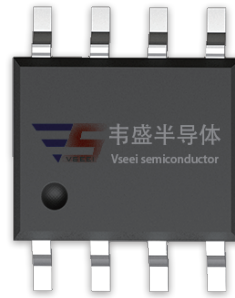
The VSM9P03 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V.

General Features

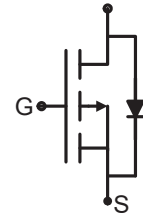
- $V_{DS} = -30V, I_D = -9.1A$
- $R_{DS(ON)} < 35m\Omega @ V_{GS} = -4.5V$
- $R_{DS(ON)} < 20m\Omega @ V_{GS} = -10V$
- High power and current handling capability
- Lead free product is acquired
- Surface mount package

Application

- Battery Switch
- Load switch
- Power management



SOP-8



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM9P03-S8	VSM9P03	SOP-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_J = 150^\circ C$)	I_D	$T_C = 25^\circ C$	-11
		$T_C = 70^\circ C$	-9
		$T_A = 25^\circ C$	-9.1
		$T_A = 70^\circ C$	-7.2
Drain Current-Pulsed ^(Note 1)	I_{DM}	-50	A
Maximum Power Dissipation	P_D	3.1	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

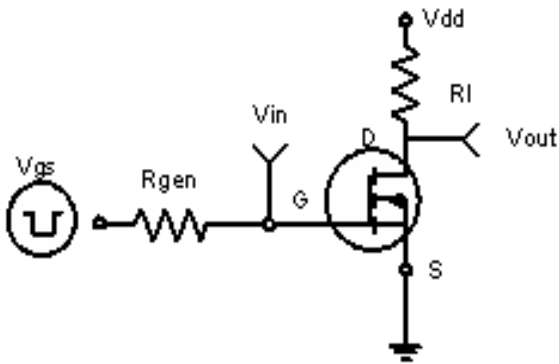
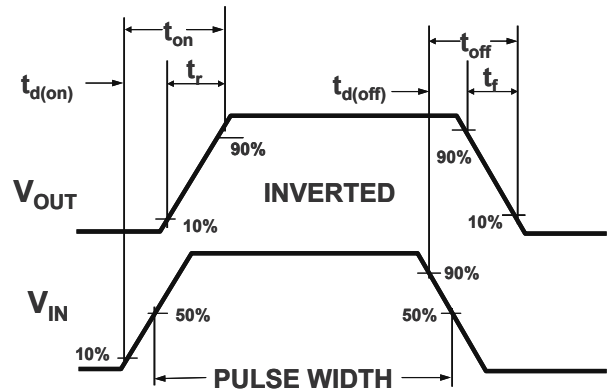
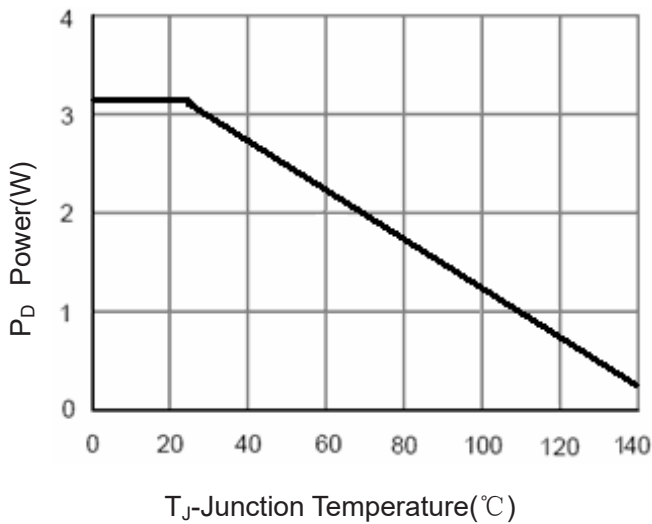
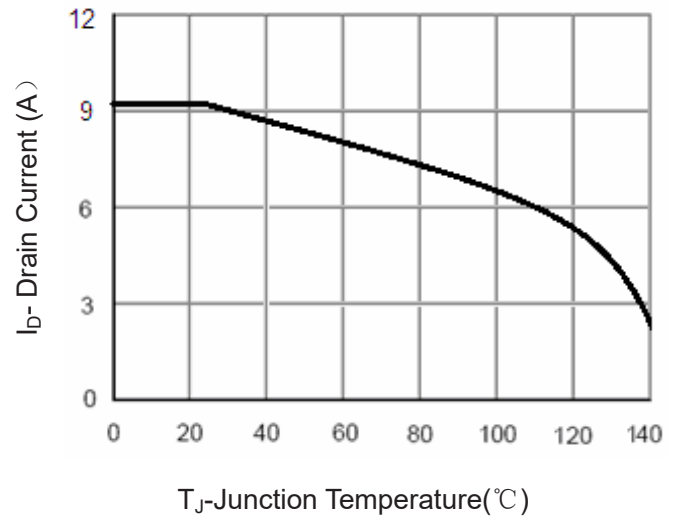
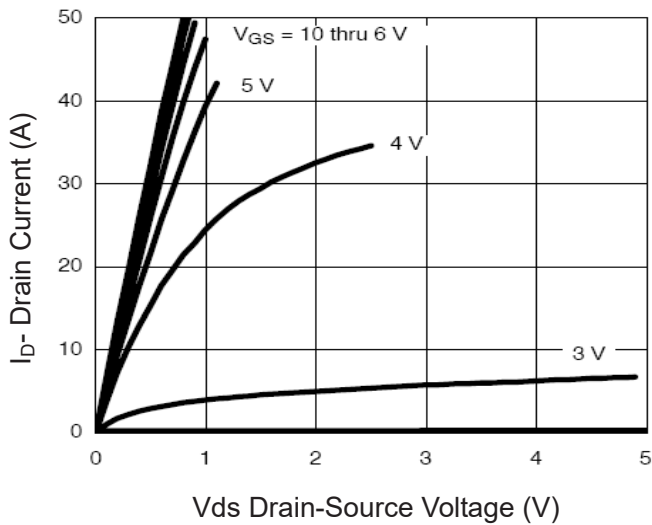
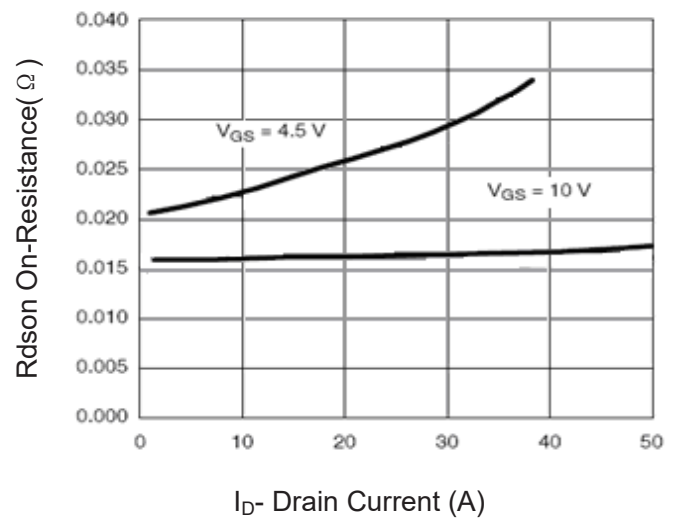
Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	40	$^\circ C/W$
Thermal Resistance, Junction-to-Lead ^(Note 2)	$R_{\theta JL}$	24	$^\circ C/W$

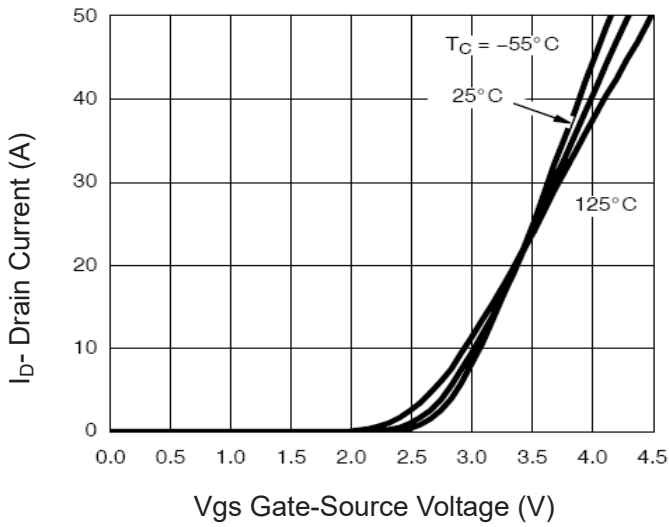
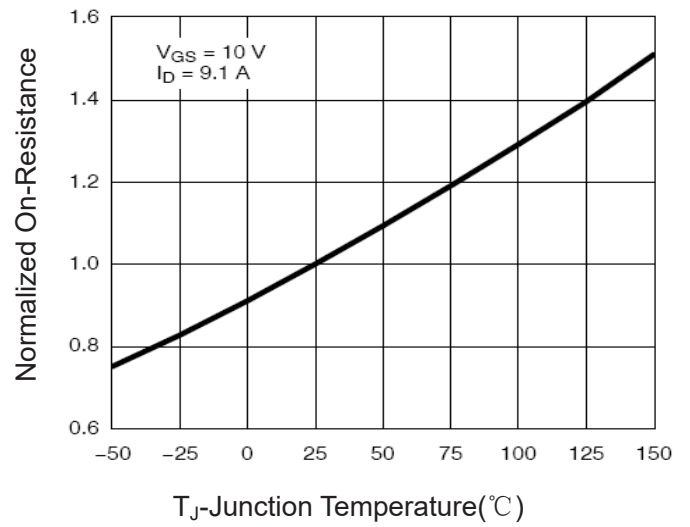
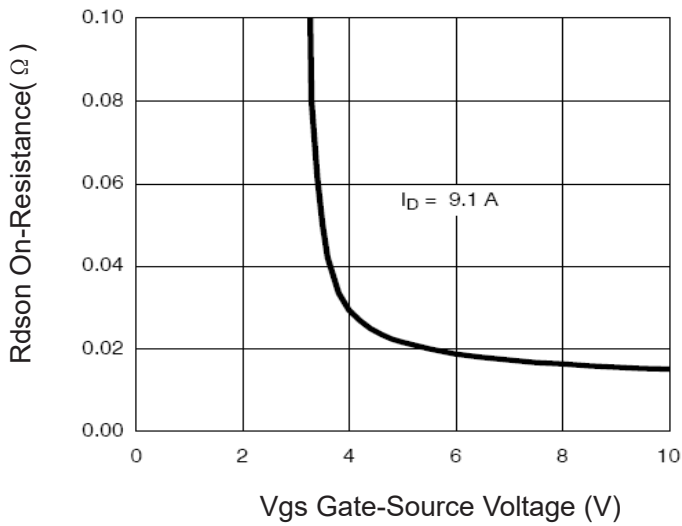
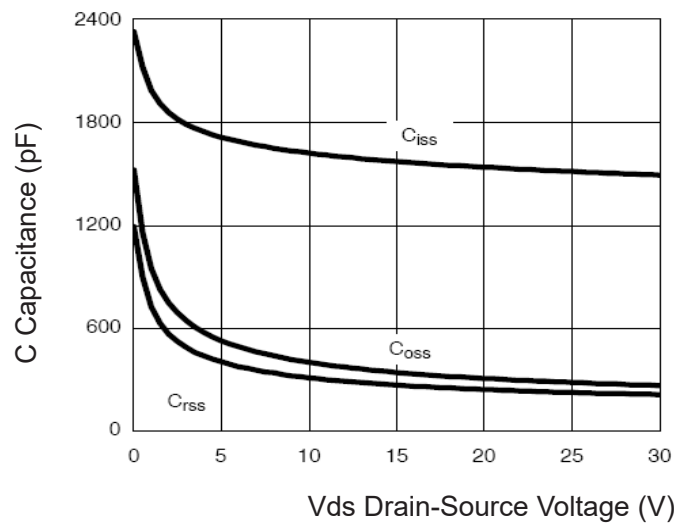
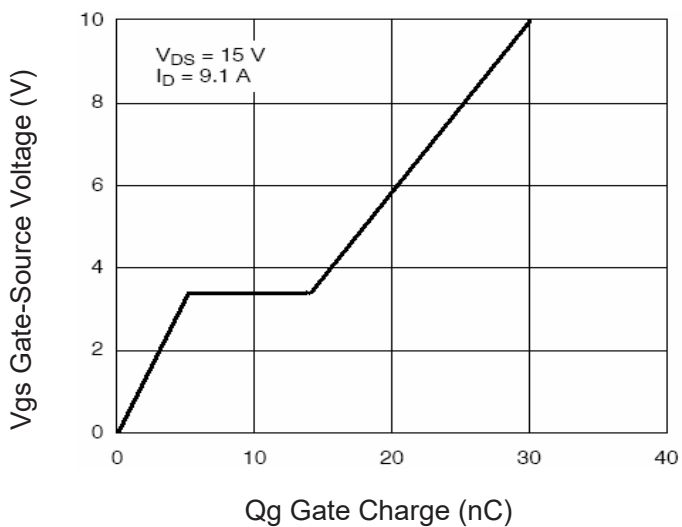
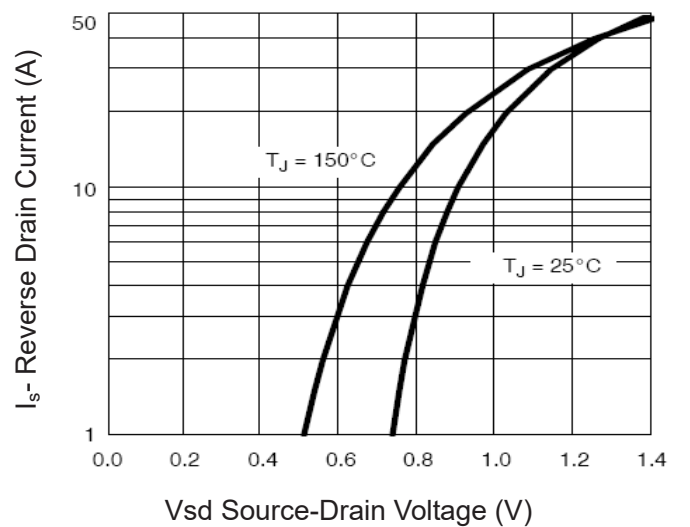
Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

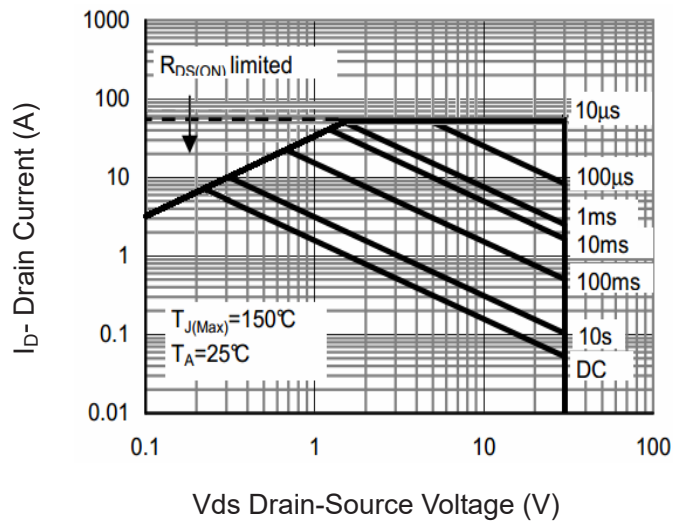
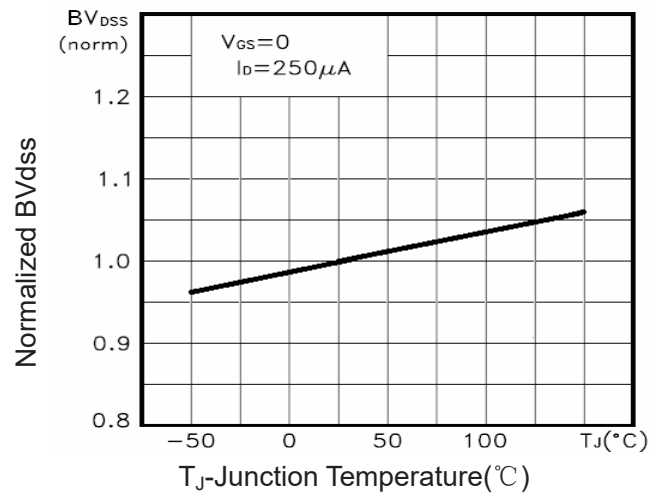
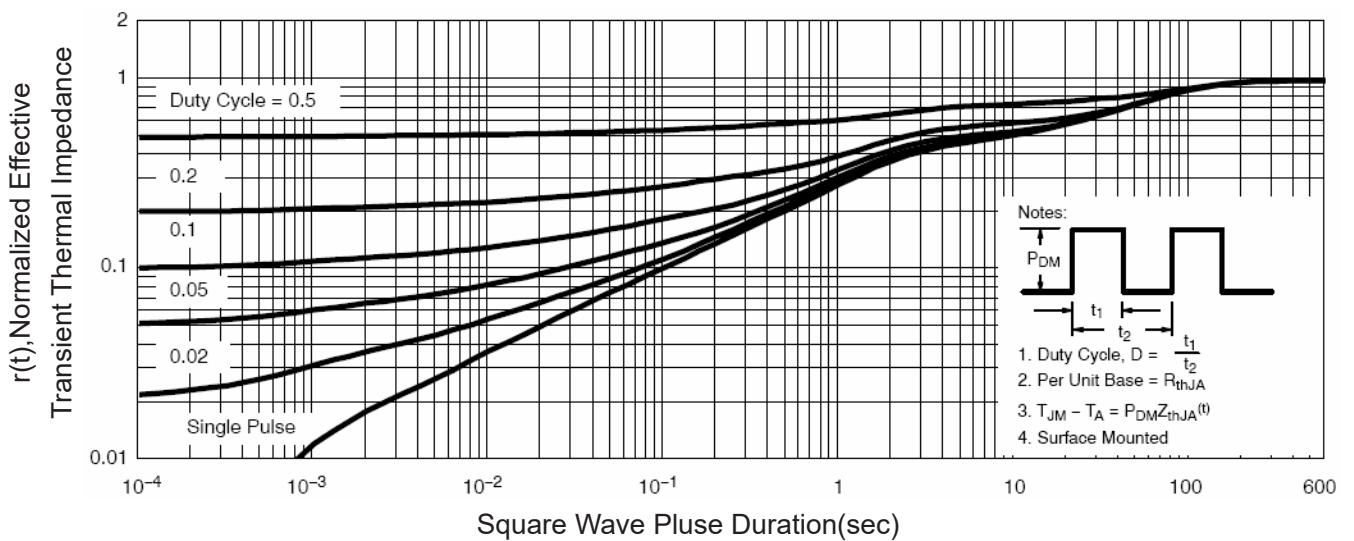
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-33	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.5	-3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-9.1A$	-	16	20	$m\Omega$
		$V_{GS}=-4.5V, I_D=-6.9A$	-	21	35	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS}=-15V, I_D=-9.1A$	10	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V,$ $F=1.0MHz$	-	1600	-	PF
Output Capacitance	C_{oss}		-	350	-	PF
Reverse Transfer Capacitance	C_{riss}		-	300	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-15V, I_D=-1A,$ $V_{GS}=-10V, R_{GEN}=6\Omega$	-	10	-	nS
Turn-on Rise Time	t_r		-	15	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	110	-	nS
Turn-Off Fall Time	t_f		-	70	-	nS
Total Gate Charge	Q_g	$V_{DS}=-15V, I_D=-9.1A$ $V_{GS}=-10V$	-	30	-	nC
Gate-Source Charge	Q_{gs}		-	5.5	-	nC
Gate-Drain Charge	Q_{gd}		-	8	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=-9.1A$	-	-	-1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10s$ thermal resistance rating. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

Figure 1: Switching Test Circuit

Figure 2: Switching Waveforms

Figure 3 Power Dissipation

Figure 4 Drain Current

Figure 5 Output Characteristics

Figure 6 Drain-Source On-Resistance


Figure 7 Transfer Characteristics

Figure 8 Drain-Source On-Resistance

Figure 9 Rdson vs Vgs

Figure 10 Capacitance vs Vds

Figure 11 Gate Charge

Figure 12 Source- Drain Diode Forward


Figure 13 Safe Operation Area

Figure 14 BV_{DS} vs Junction Temperature

Figure 15 Normalized Maximum Transient Thermal Impedance