

### Description

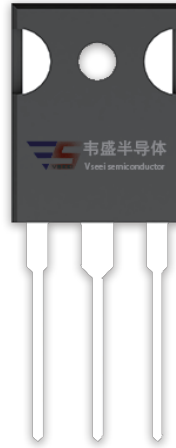
The VST04N008 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of  $R_{DS(on)}$  and  $Q_g$ . This device is ideal for high-frequency switching and synchronous rectification.

### General Features

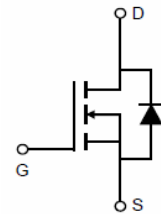
- $V_{DS} = 40V, I_D = 350A$   
 $R_{DS(on)} = 0.8m\Omega$  (typical) @  $V_{GS} = 10V$
- Excellent gate charge x  $R_{DS(on)}$  product(FOM)
- Very low on-resistance  $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

### Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



TO-247



Schematic Diagram

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST04N008-T7	VST04N008	TO-247	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous (Silicon Limited)	$I_D$	350	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	247	A
Pulsed Drain Current	$I_{DM}$	1400	A
Maximum Power Dissipation	$P_D$	500	W
Derating factor		3.33	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	1800	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

### Thermal Characteristic

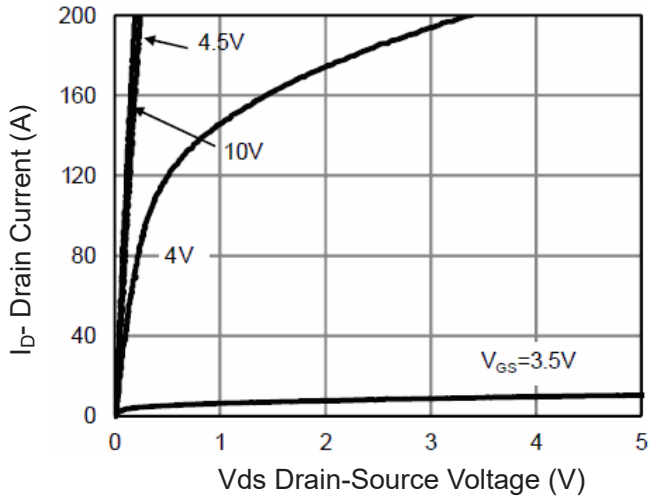
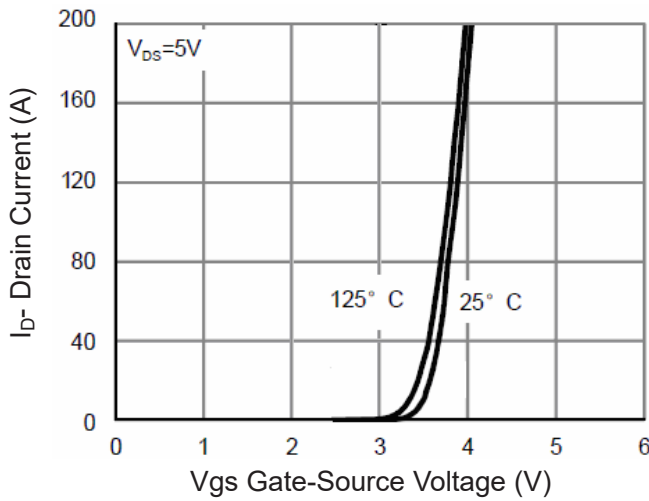
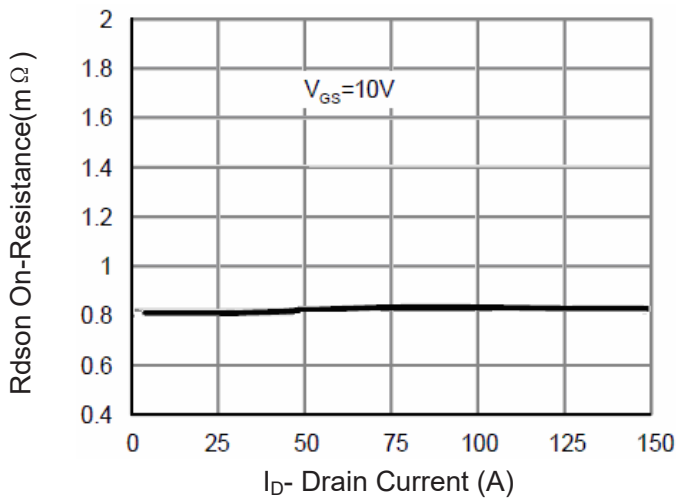
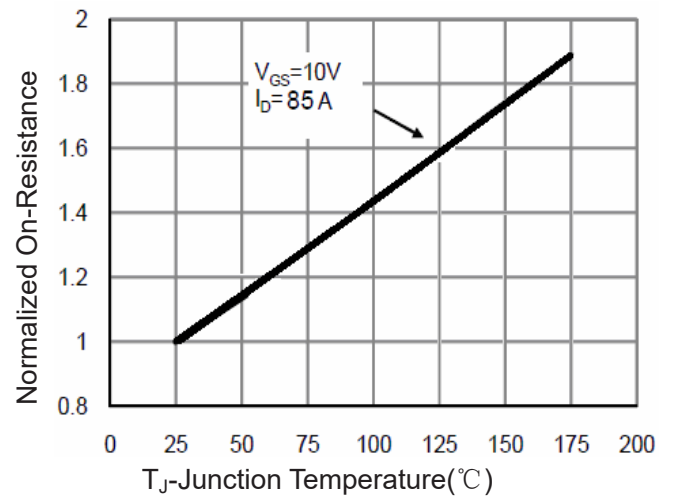
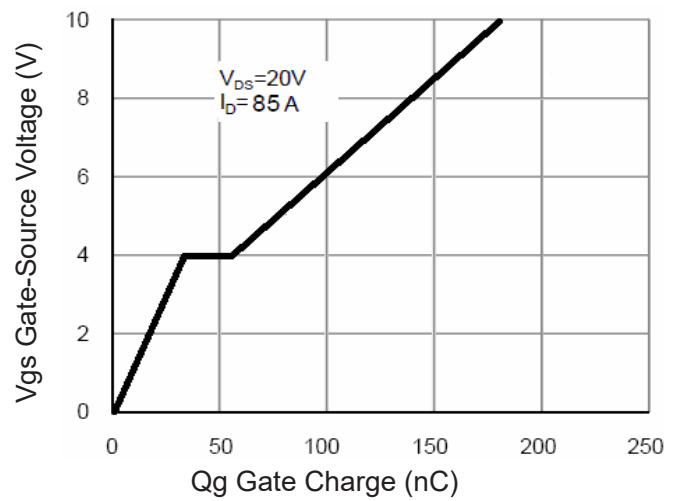
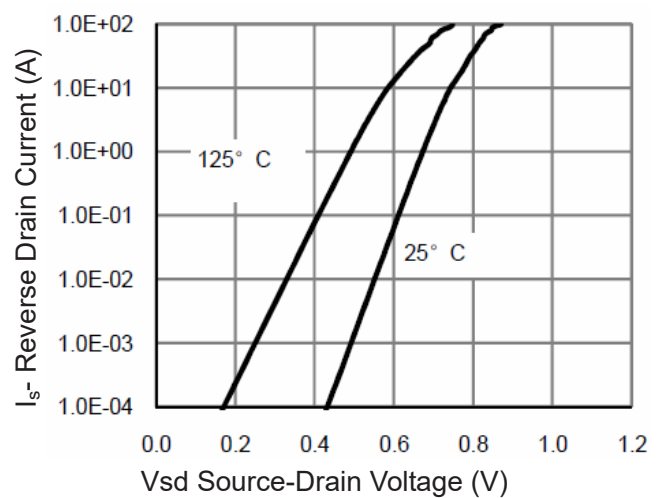
Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	0.3	$^\circ C/W$
--	-----------------	-----	--------------

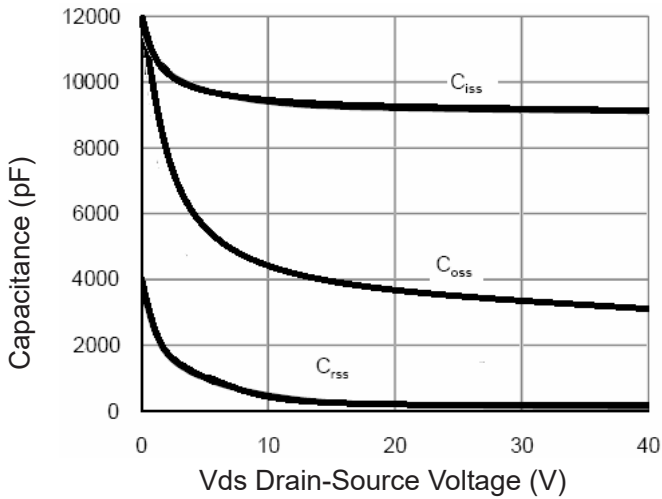
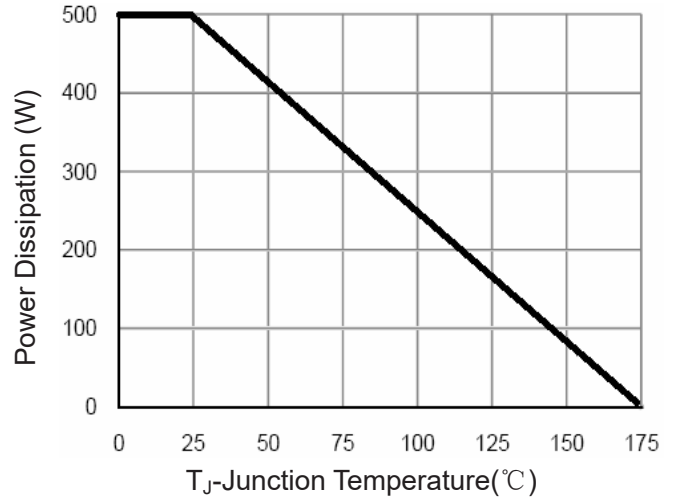
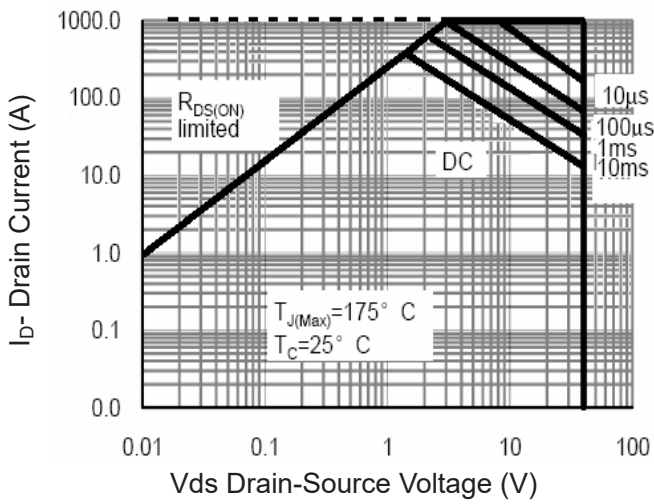
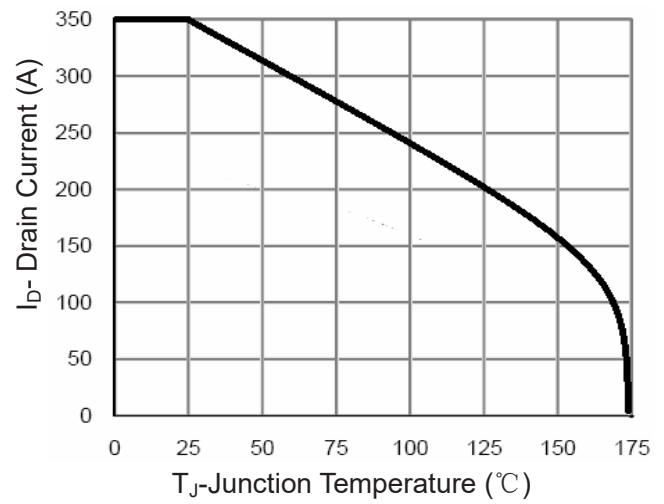
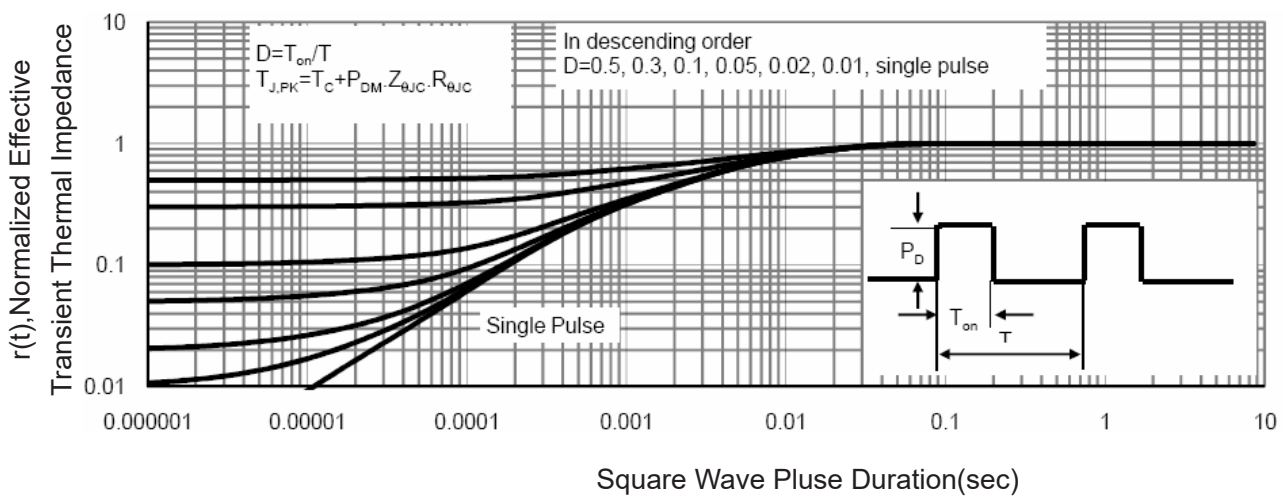
**Electrical Characteristics ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	40		-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	2.5	3.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=85A$	-	0.8	1.1	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=85A$	-	100	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	$C_{iss}$	$V_{DS}=20V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	9500	-	PF
Output Capacitance	$C_{oss}$		-	3860	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	120	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, I_D=85A$ $V_{GS}=10V, R_G=1.6\Omega$	-	26	-	nS
Turn-on Rise Time	$t_r$		-	14	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	110	-	nS
Turn-Off Fall Time	$t_f$		-	17	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=20V, I_D=85A,$ $V_{GS}=10V$	-	177	-	nC
Gate-Source Charge	$Q_{gs}$		-	32		nC
Gate-Drain Charge	$Q_{gd}$		-	26		nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_S=85A$	-		1.2	V
Diode Forward Current	$I_S$		-	-	350	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}, I_F = I_S$ $di/dt = 100A/\mu s$ (Note 3)	-		66	nS
Reverse Recovery Charge	$Q_{rr}$		-		240	nC

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition :  $T_J=25^{\circ}\text{C}, V_{DD}=20V, V_G=10V, L=0.5\text{mH}, R_G=25\Omega$

**Typical Electrical and Thermal Characteristics**

**Figure 1 Output Characteristics**

**Figure 2 Transfer Characteristics**

**Figure 3 Rdson- Drain Current**

**Figure 4 Rdson-Junction Temperature**

**Figure 5 Gate Charge**

**Figure 6 Source- Drain Diode Forward**


**Figure 7 Capacitance vs Vds**

**Figure 9 Power De-rating**

**Figure 8 Safe Operation Area**

**Figure 10 Current De-rating**

**Figure 11 Normalized Maximum Transient Thermal Impedance**