Description

These N-Channel enhancement mode power field effect transistors are using split gate trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and with stand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

- 40V,120A, $R_{DS(on),max}$ =2.5mΩ@V_{GS} = 10V
- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- Green device available

Applications

- Motor Drives
- UPS
- DC-DC Converter

Product Summary

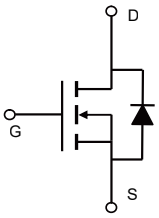
V_{DSS}	40V
$R_{DS(on),max}$@ V_{GS}=10V	2.5mΩ
I_D	120A

Pin Configuration

TO-251

TO-252

TO-220C



Schematic

Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	40	V
Continuous drain current (T_C = 25°C)[1]	I_D	120	A
Continuous drain current (T_C = 100°C)		81	A
Pulsed drain current[2]	I_{DM}	360	A
Gate-Source voltage	V_{GSS}	±18	V
Avalanche energy[3]	E_{AS}	306	mJ
Power Dissipation (T_C = 25°C)	P_D	57.6	W
Storage Temperature Range	T_{STG}	-55 to +150	°C
Operating Junction Temperature Range	T_J	-55 to +150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.17	°C/W

Package Marking and Ordering Information

Device	Device Package	Marking
VST04N025-T1	TO-251	VST04N025-T1
VST04N025-T2	TO-252	VST04N025-T2
VST04N025-TC	TO-220C	VST04N025-TC

Electrical Characteristics

T_J = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0 V, I_D=250uA	40	---	---	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	1.0	1.5	2.2	V
Drain-source leakage current	I_{DSS}	V_{DS}=40 V, V_{GS}=0V, T_J = 25°C	---	---	1	μA
Gate leakage current, Forward	I_{GSSF}	V_{GS}=18 V, V_{DS}=0 V	---	---	100	nA
Gate leakage current, Reverse	I_{GSSR}	V_{GS}=-18 V, V_{DS}=0 V	---	---	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=50 A	---	2.2	2.5	mΩ
		V_{GS}=4.5 V, I_D=20 A	---	2.9	5	mΩ
Forward transconductance	g_{fs}	V_{DS} =10V , I_D=20A	---	125	---	S
Dynamic characteristics						
Input capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, F = 1MHz	---	3550	---	pF
Output capacitance	C_{oss}		---	1790	---	
Reverse transfer capacitance	C_{rss}		---	178	---	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 15V,V_{GS}=10V, I_D = 20A R_G=15Ω	---	11	---	ns
Rise time	t_r		---	10	---	
Turn-off delay time	$t_{d(off)}$		---	160	---	
Fall time	t_f		---	41	---	
Gate charge characteristics						
Gate to source charge	Q_{gs}	V_{DS}=15V, I_D=15A, V_{GS}= 10 V	---	7.7	---	nC
Gate to drain charge	Q_{gd}		---	7.9	---	
Gate charge total	Q_g		---	50	---	
Drain-Source diode characteristics and Maximum Ratings						
Continuous Source Current	I_S		---	---	120	A
Pulsed Source Current[4]	I_{SM}		---	---	360	A
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=50A, T_J=25℃	---	0.85	1.2	V
Reverse Recovery Time	t_{rr}	I_S=I_F, di/dt=100A/us, T_J=25℃ [5]	---	---	96	ns
Reverse Recovery Charge	Q_{rr}		---	---	76.8	nC

Notes:

1: The maximum junction current rating is package limited.

2: Repetitive Rating: Pulse width limited by maximum junction temperature.

3: V_{DD}=30V, V_{GS}=10V, L=0.5mH, I_{AS}=35A, R_G=25Ω, Starting T_J=25℃.

4: Pulse Test：Pulse Width ≤300 μs, Duty Cycle≤2%.

5: Guaranteed by design, not subject to production.

Electrical Characteristics Diagrams

Fig 1: Output Characteristics

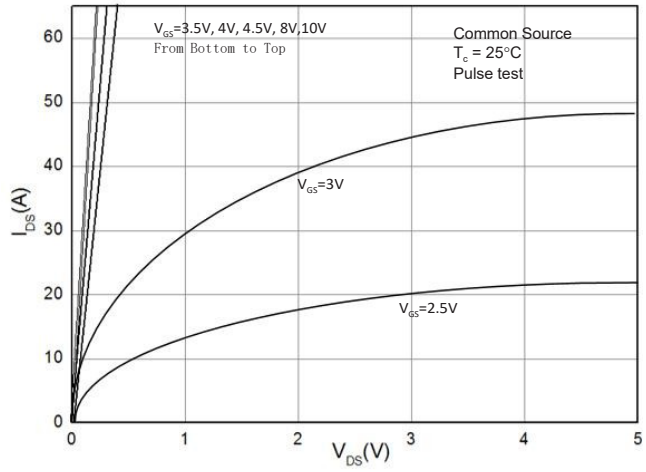


Fig 2: Transfer Characteristics

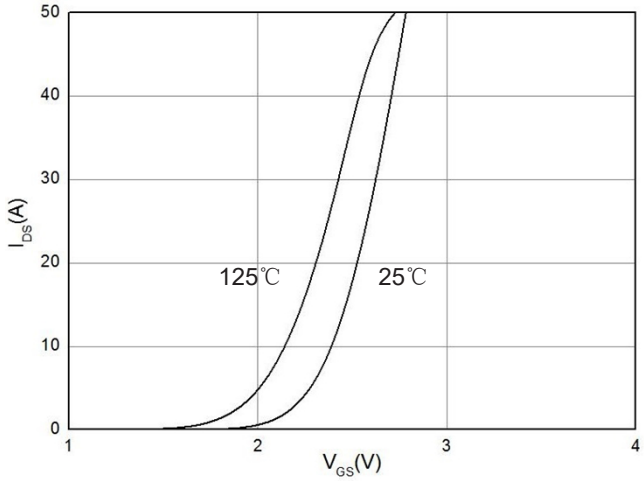


Figure 3. Capacitance Characteristics

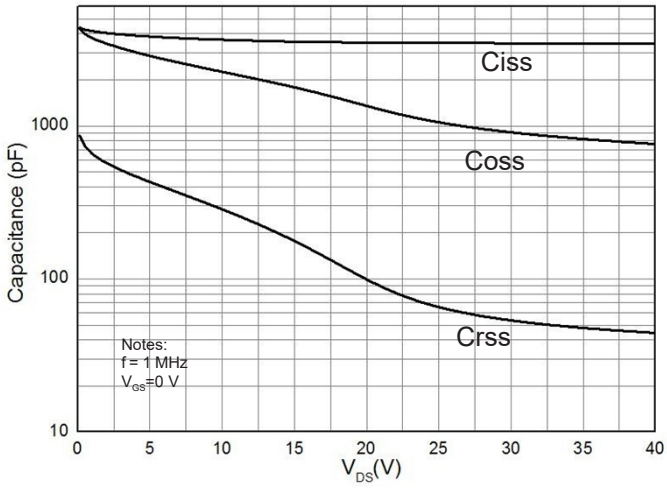


Figure 4. Gate Charge Waveform

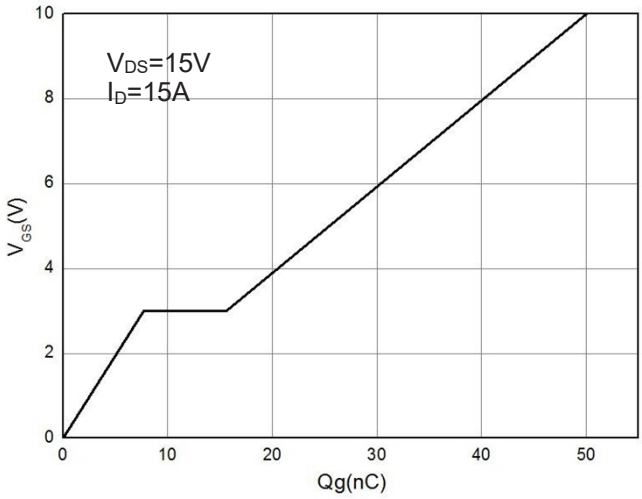


Figure 5. Body-Diode Characteristics

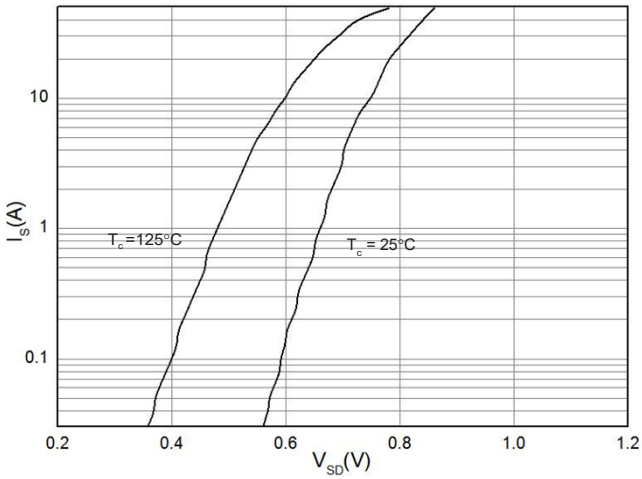


Figure 6. Rdson-Drain Current

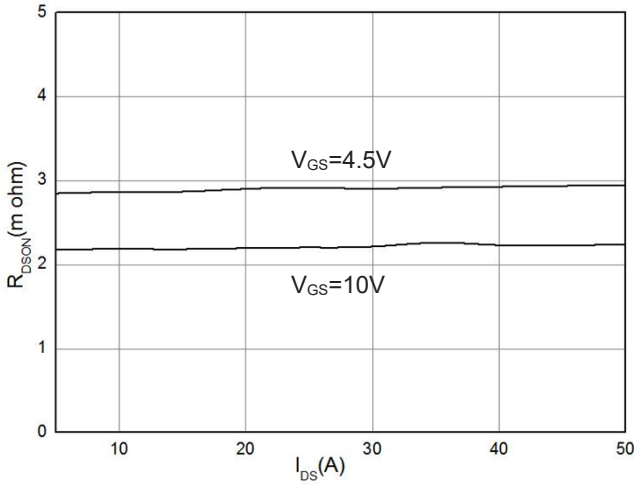


Fig 7: Rds(on) vs Gate Voltage

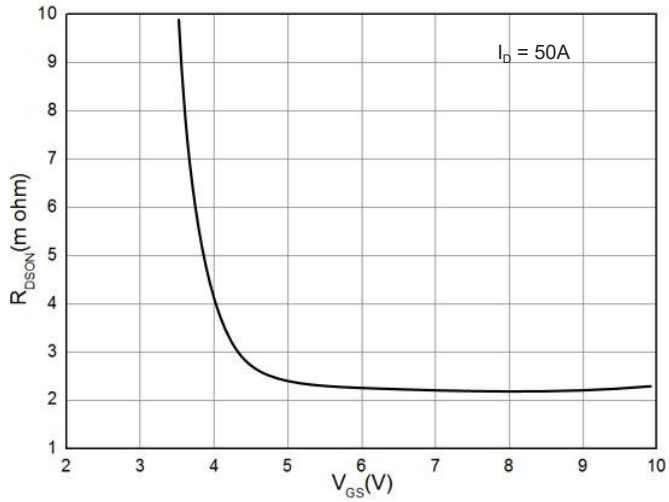


Fig 8: Rdson-Junction Temperature(℃)

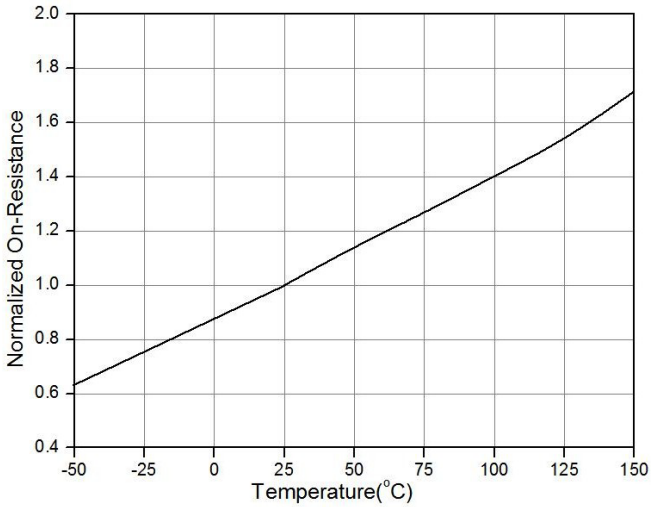


Figure 9. BVdss vs. Junction temperature

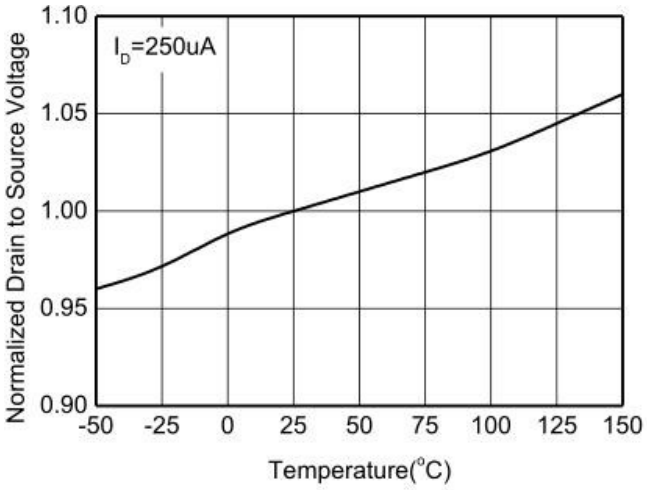


Figure 10. Maximum Safe Operating Area

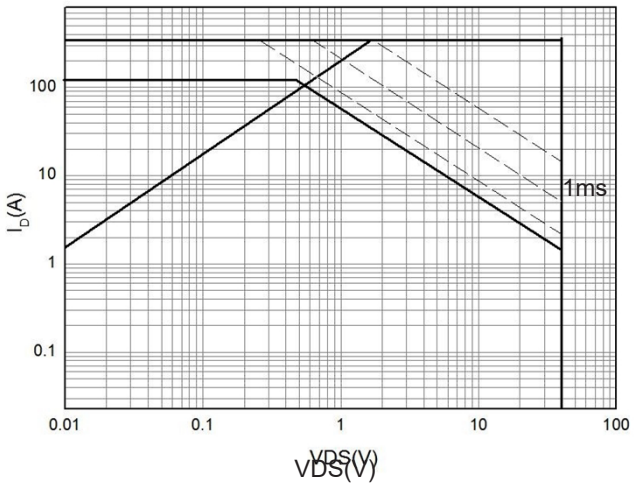
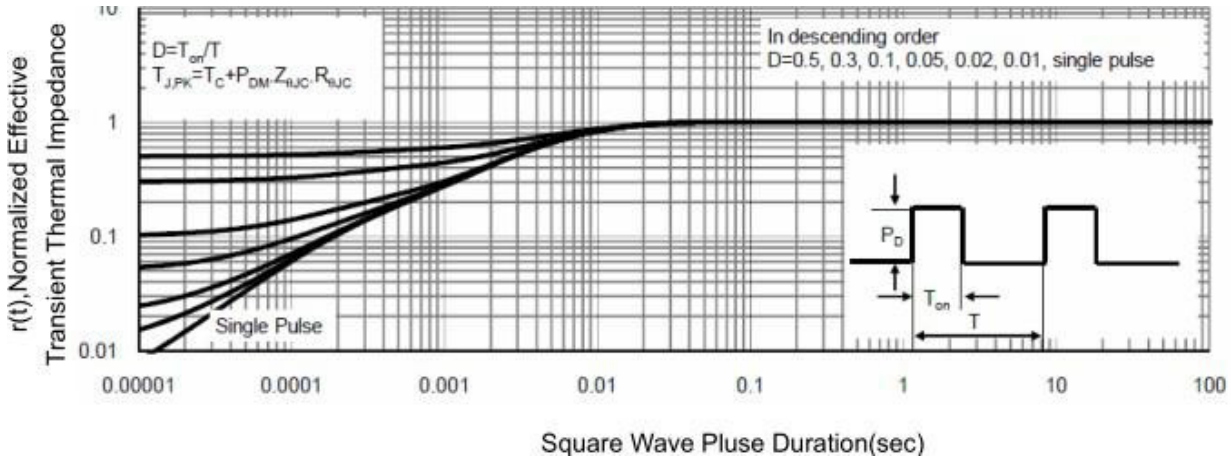


Figure 11. Normalized Maximum Transient Thermal Impedance (RthJC)



Test Circuit & Waveform

Figure 12. Gate Charge Test Circuit & Waveform

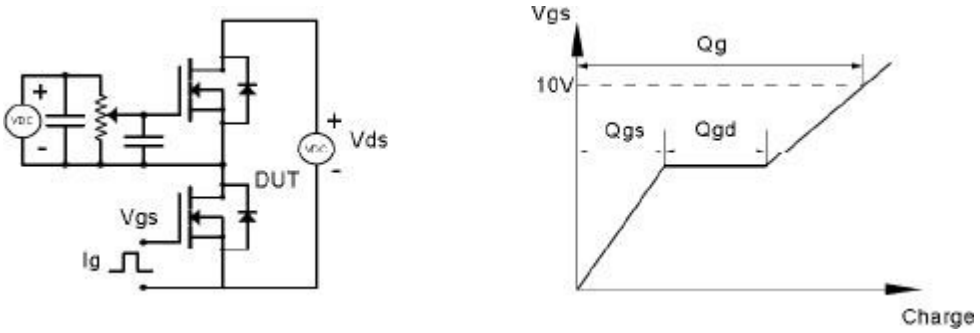


Figure 13. Resistive Switching Test Circuit & Waveforms

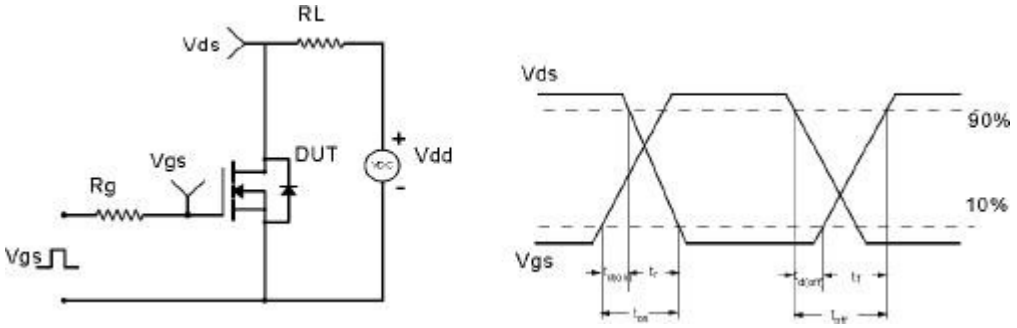


Figure 14. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

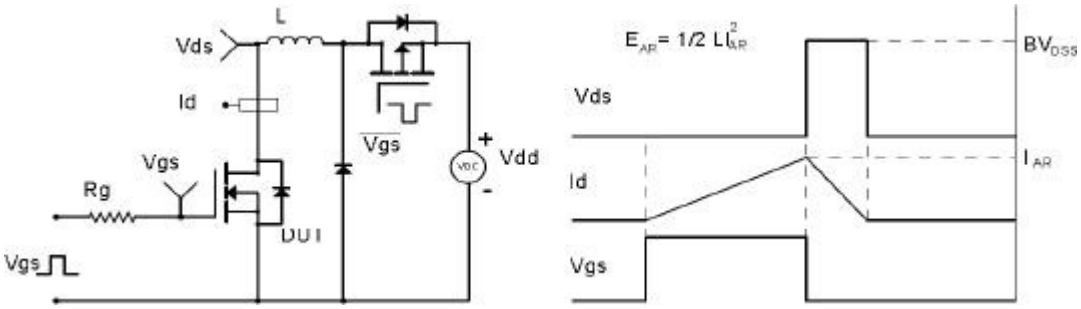


Figure 15. Diode Recovery Circuit & Waveform