

Description

The VST08N022 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

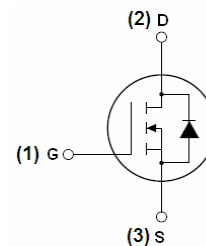
- $V_{DS} = 85V, I_D = 250A$
 $R_{DS(ON)} < 2.6m\Omega @ V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



TO-220C



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST08N022-TC	VST08N022	TO-220C	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	85	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	250	A
Drain Current-Continuous($T_C = 100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	180	A
Pulsed Drain Current	I_{DM}	1000	A
Maximum Power Dissipation	P_D	300	W
Derating factor		2	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	2000	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

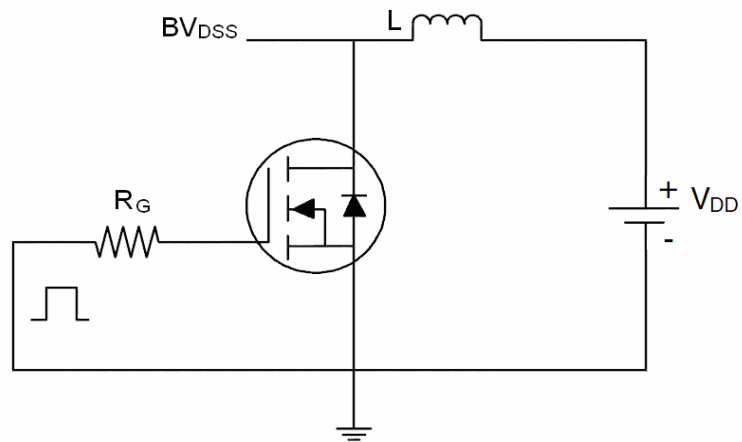
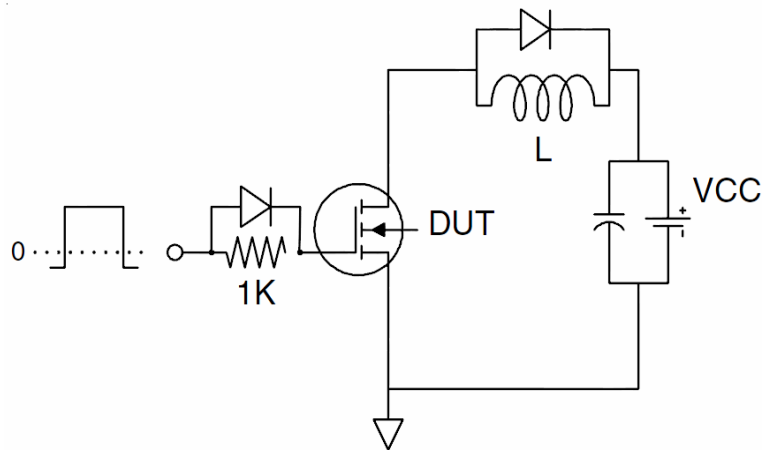
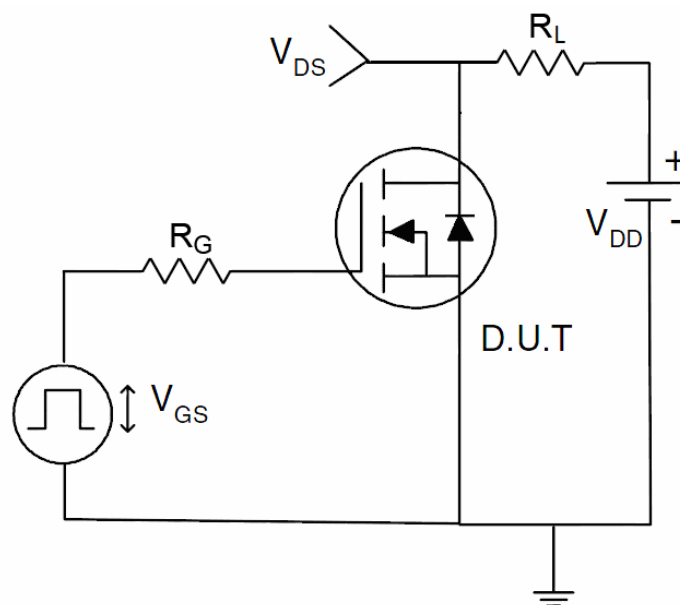
Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.5	°C/W
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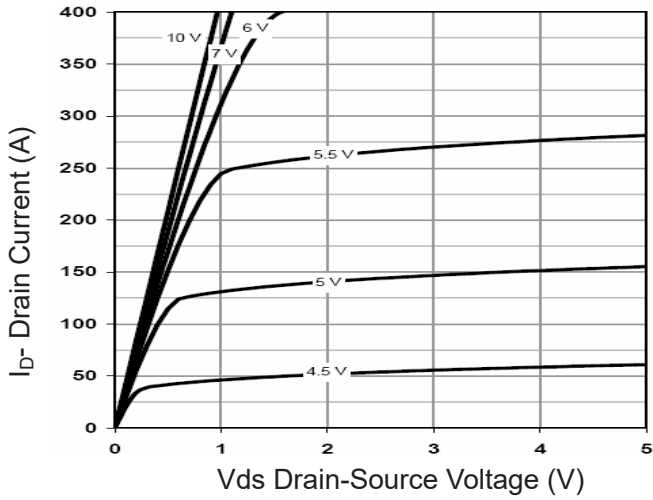
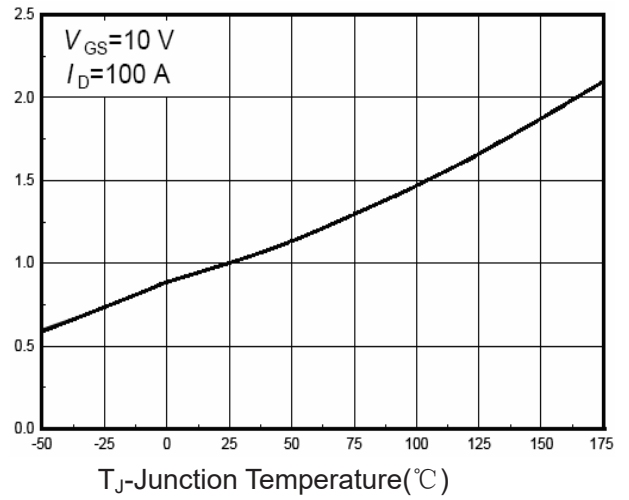
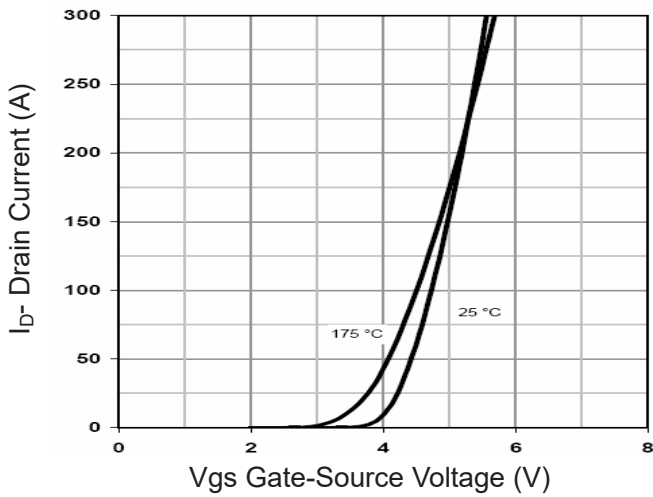
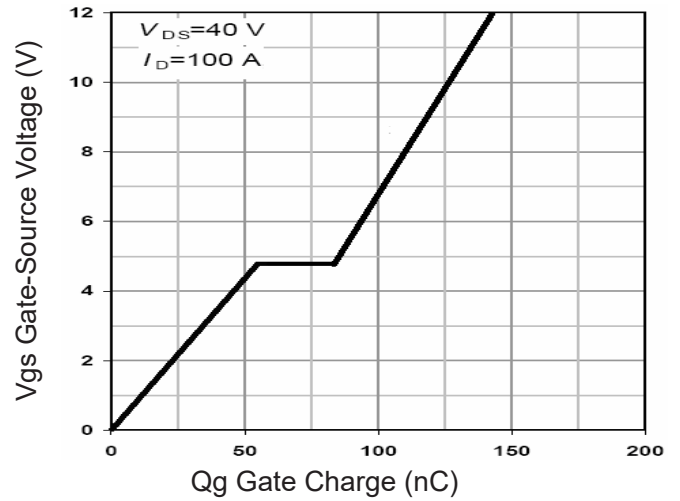
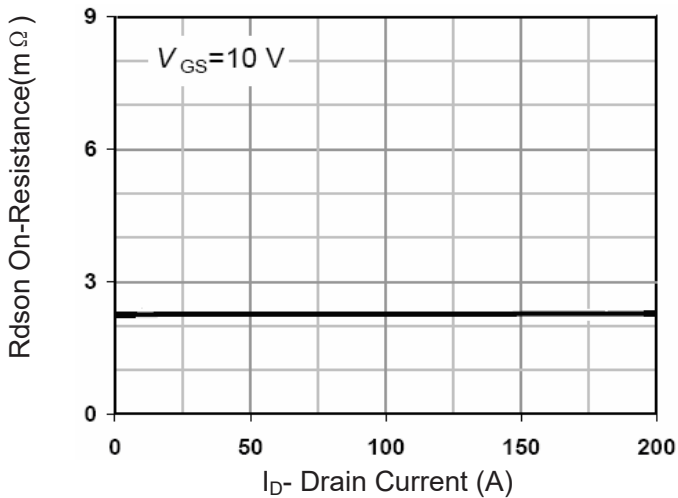
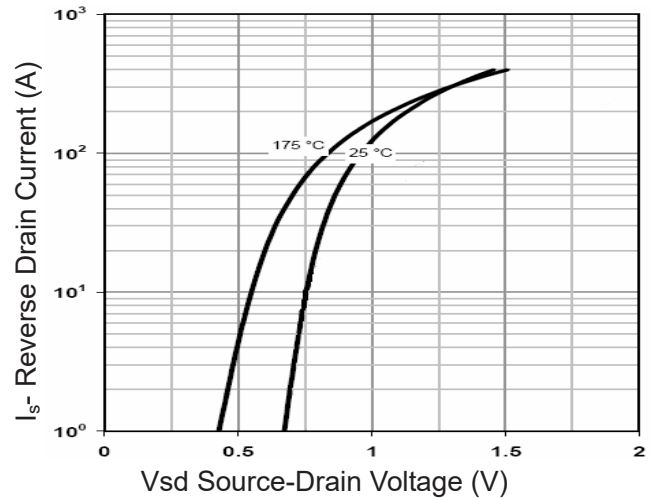
Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	85		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=85V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5	3.5	4.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=100A$	-	2.2	2.6	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=100A$	-	90	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=40V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	10700	-	PF
Output Capacitance	C_{oss}		-	1700	-	PF
Reverse Transfer Capacitance	C_{rss}		-	76	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=40V, I_D=100A$ $V_{GS}=10V, R_G=1.6\Omega$	-	28	-	nS
Turn-on Rise Time	t_r		-	73	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	86	-	nS
Turn-Off Fall Time	t_f		-	33	-	nS
Total Gate Charge	Q_g	$V_{DS}=40V, I_D=100A,$ $V_{GS}=10V$	-	142		nC
Gate-Source Charge	Q_{gs}		-	56		nC
Gate-Drain Charge	Q_{gd}		-	24		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_F=I_S$	-		1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	250	A
Reverse Recovery Time	t_{rr}	$T_J=25^\circ\text{C}, I_F=I_S$	-	115		nS
Reverse Recovery Charge	Q_{rr}	$di/dt=100A/\mu s$ ^(Note 3)	-	320		nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^\circ\text{C}, V_{DD}=42.5V, V_G=10V, L=0.5mH, R_G=25\Omega$

Test Circuit**1) E_{AS} test Circuit****2) Gate charge test Circuit****3) Switch Time Test Circuit**

Typical Electrical and Thermal Characteristics

Figure 1 Output Characteristics

Figure 4 Rds(on)-Junction Temperature

Figure 2 Transfer Characteristics

Figure 5 Gate Charge

Figure 3 Rds(on)- Drain Current

Figure 6 Source- Drain Diode Forward

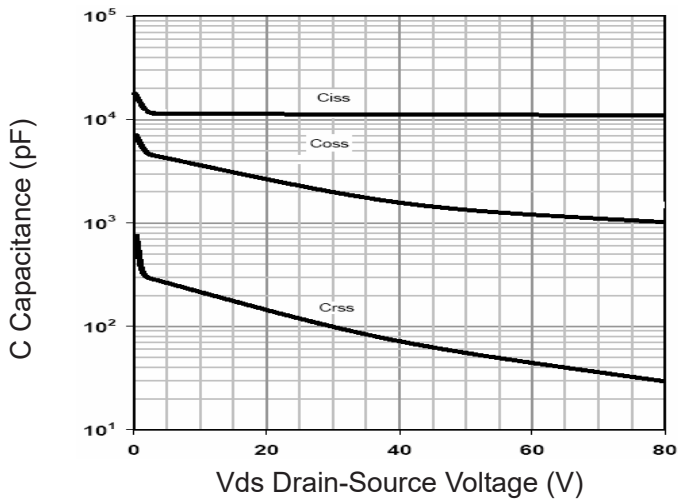


Figure 7 Capacitance vs Vds

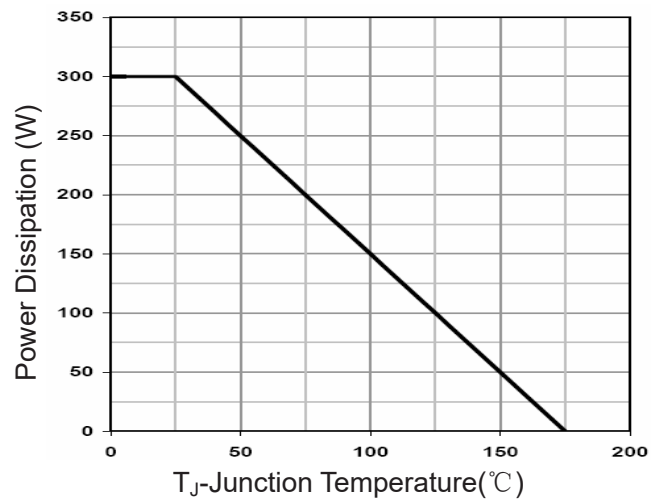


Figure 9 Power De-rating

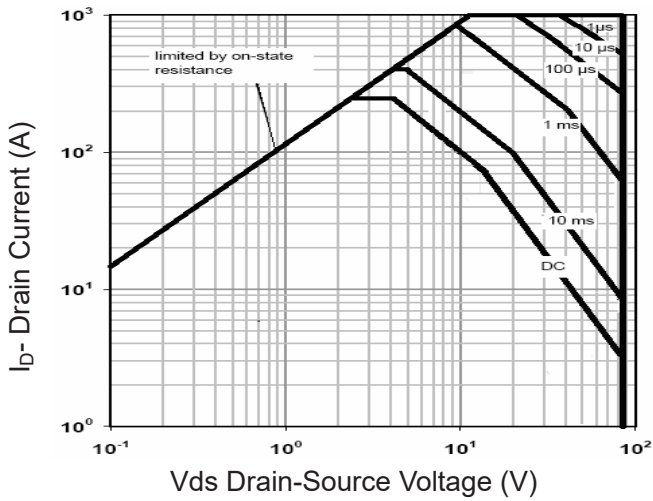


Figure 8 Safe Operation Area

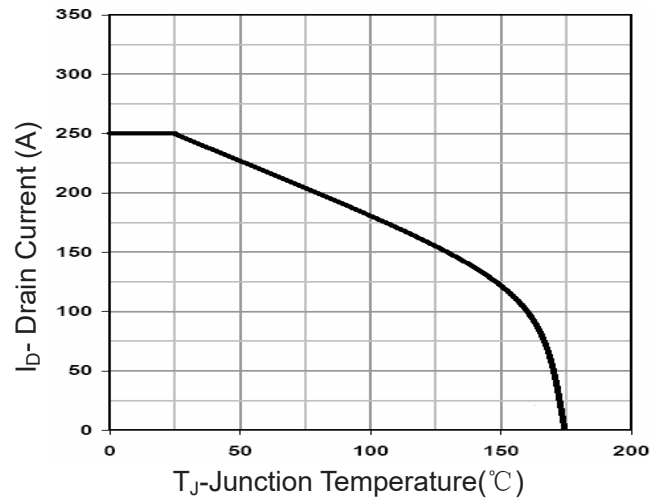


Figure 10 Current De-rating

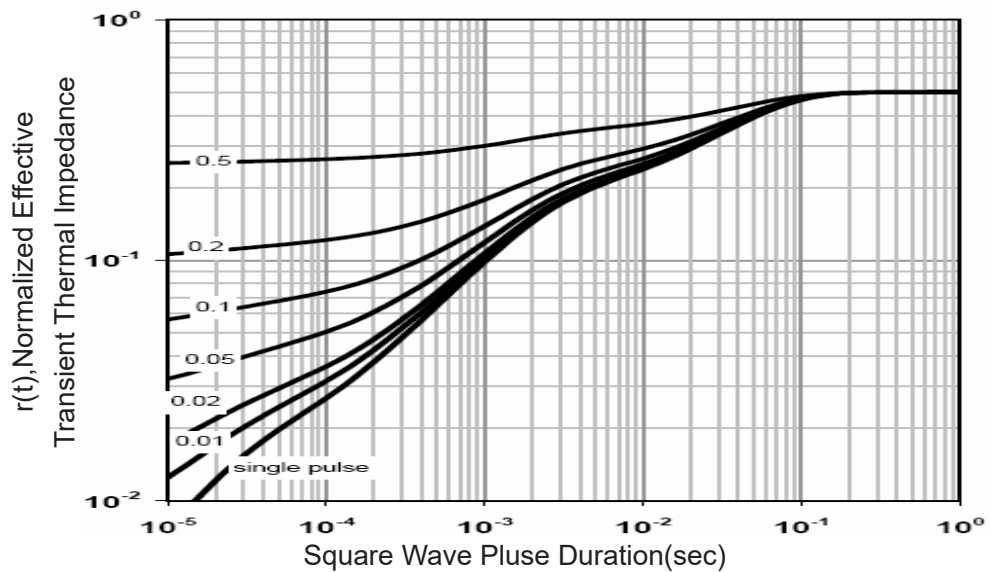


Figure 11 Normalized Maximum Transient Thermal Impedance