## Description

The VST08N050 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and $Q_g$. This device is ideal for high-frequency switching and synchronous rectification.

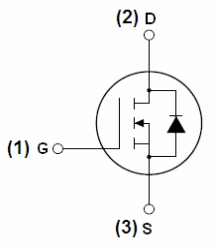
## General Features

- $V_{DS}$ =85V,$I_D$ =115A
  $R_{DS(ON)}$ <5.7mΩ @ $V_{GS}$=10V
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

## Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification


TO-263




Schematic Diagram

## Package Marking and Ordering Information

| Device Marking | Device | Device Package | Reel Size | Tape width | Quantity |
|---|---|---|---|---|---|
| VST08N050-T3 | VST08N050 | TO-263 | - | - | - |

## Absolute Maximum Ratings ($T_C$=25℃unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 85 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Drain Current-Continuous | $I_D$ | 115 | A |
| Drain Current-Continuous($T_C$=100℃) | $I_D$ (100℃) | 81.3 | A |
| Pulsed Drain Current | $I_{DM}$ | 420 | A |
| Maximum Power Dissipation | $P_D$ | 157 | W |
| Derating factor | | 1.05 | W/℃ |
| Single pulse avalanche energy (Note 5) | $E_{AS}$ | 726 | mJ |
| Operating Junction and Storage Temperature Range | $T_J$,$T_{STG}$ | -55 To 175 | ℃ |

## Thermal Characteristic

| | | | |
|---|---|---|---|
| Thermal Resistance,Junction-to-Case (Note 2) | $R_{\theta JC}$ | 0.96 | ℃/W |
| Thermal Resistance,Junction-to-Ambient (Note 2) | $R_{\theta JA}$ | 60 | ℃/W |

## Electrical Characteristics ($T_C$=25℃unless otherwise noted)

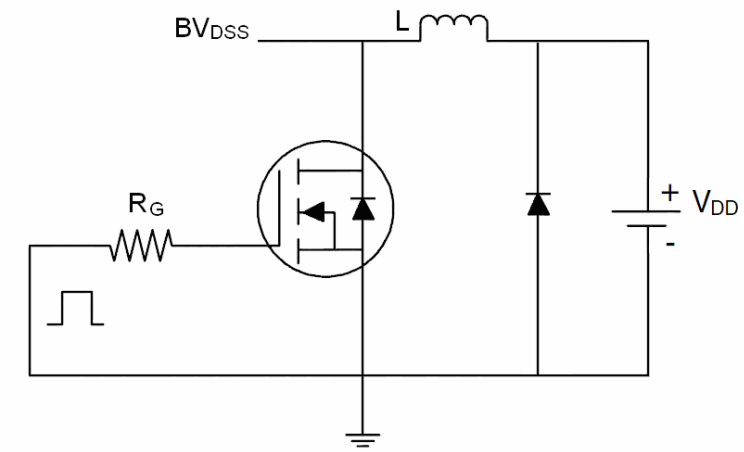
| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V $I_D$=250μA | 85 | | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=85V,$V_{GS}$=0V | - | - | 1 | μA |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V,$V_{DS}$=0V | - | - | ±100 | nA |
| **On Characteristics** (Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,$I_D$=250μA | 2.0 | 2.9 | 4.0 | V |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=55A | - | 5.0 | 5.7 | mΩ |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$=10V,$I_D$=55A | - | 47 | - | S |
| **Dynamic Characteristics** (Note4) | | | | | | |
| Input Capacitance | $C_{lss}$ | $V_{DS}$=40V,$V_{GS}$=0V, F=1.0MHz | - | 3841 | - | PF |
| Output Capacitance | $C_{oss}$ | | - | 651.7 | - | PF |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 32.7 | - | PF |
| **Switching Characteristics** (Note 4) | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$=40V,$I_D$=55A $V_{GS}$=10V,$R_G$=3Ω | - | 15.6 | - | nS |
| Turn-on Rise Time | $t_r$ | | - | 32.7 | - | nS |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 24.2 | - | nS |
| Turn-Off Fall Time | $t_f$ | | - | 15.1 | - | nS |
| Total Gate Charge | $Q_g$ | $V_{DS}$=40V,$I_D$=55A, $V_{GS}$=10V | - | 59.4 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 16.5 | | nC |
| Gate-Drain Charge | $Q_{gd}$ | | - | 12.3 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| Diode Forward Voltage (Note 3) | $V_{SD}$ | $V_{GS}$=0V,$I_S$=115A | - | | 1.2 | V |
| Diode Forward Current (Note 2) | $I_S$ | | - | - | 115 | A |
| Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25°C, $I_F$ = 55 di/dt = 100A/μs (Note3) | - | 64.3 | | nS |
| Reverse Recovery Charge | Qrr | | - | 152.7 | | nC |

## Notes:

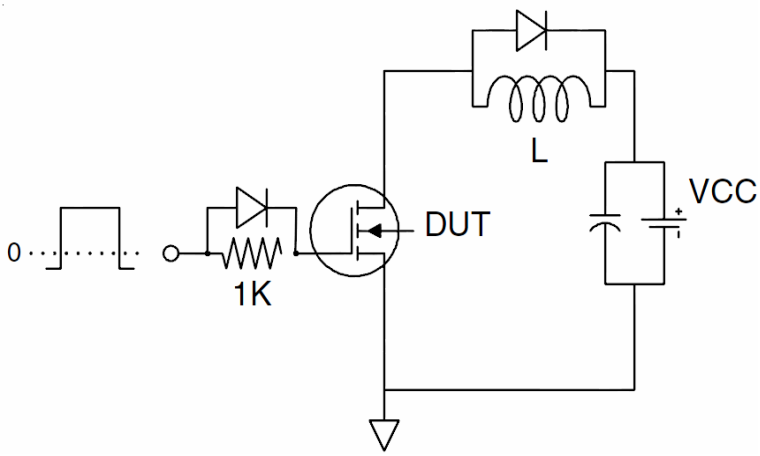
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25° C. The Power dissipation PDSM is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition : Tj=25℃,$V_{DD}$=42.5V,$V_G$=10V,L=0.5mH,Rg=25Ω

## Test Circuit

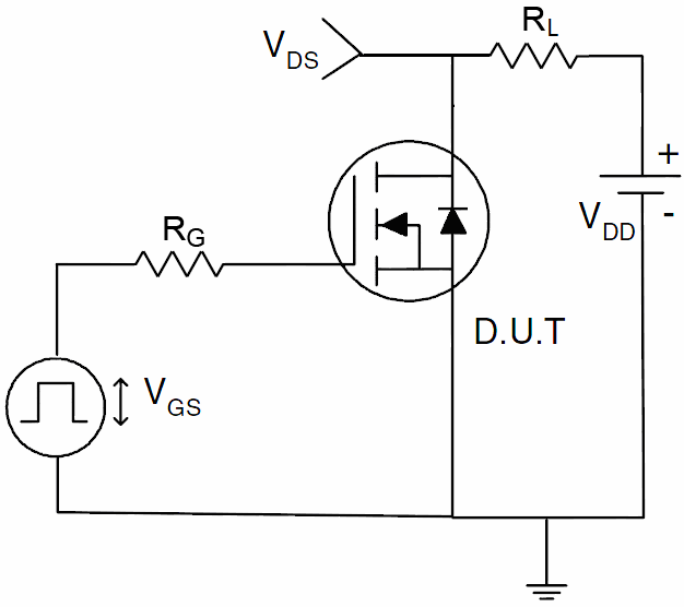
### 1) $E_{AS}$ test Circuit




### 2) Gate charge test Circuit




### 3) Switch Time Test Circuit



## Typical Electrical and Thermal Characteristics

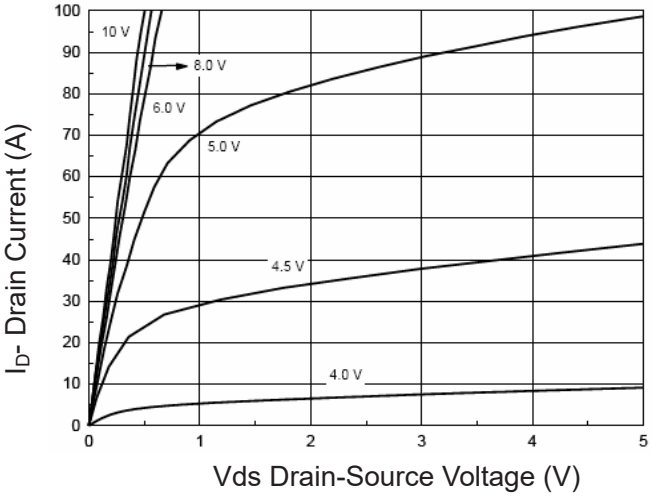



**Figure 1 Output Characteristics**

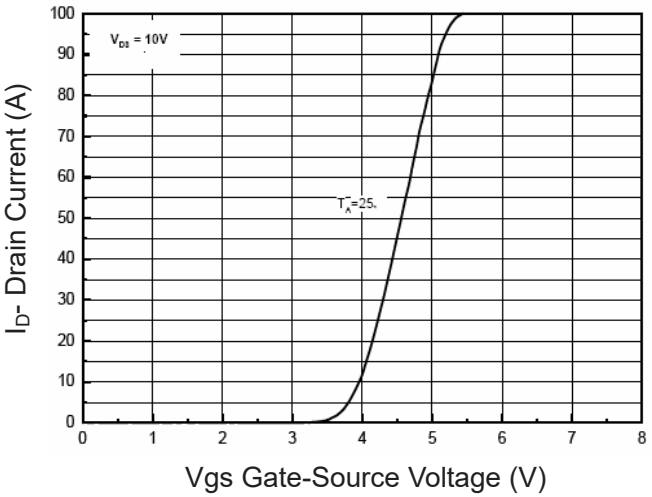



**Figure 2 Transfer Characteristics**

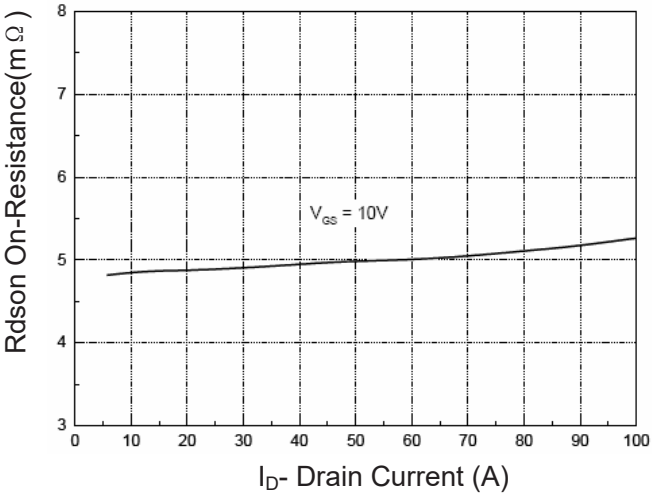



**Figure 3 Rdson- Drain Current**

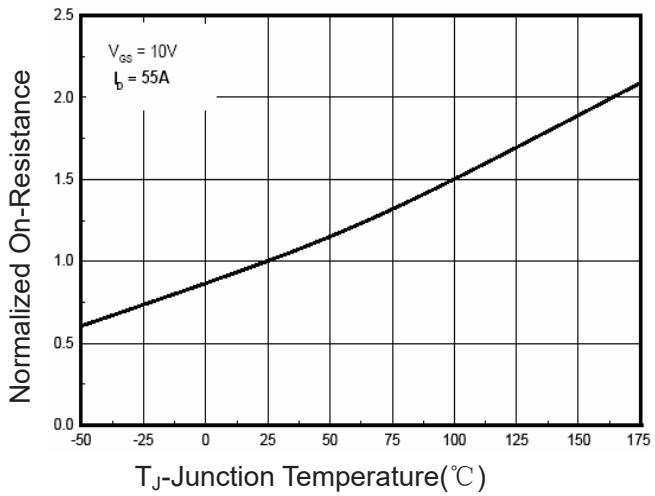



**Figure 4 Rdson-JunctionTemperature**

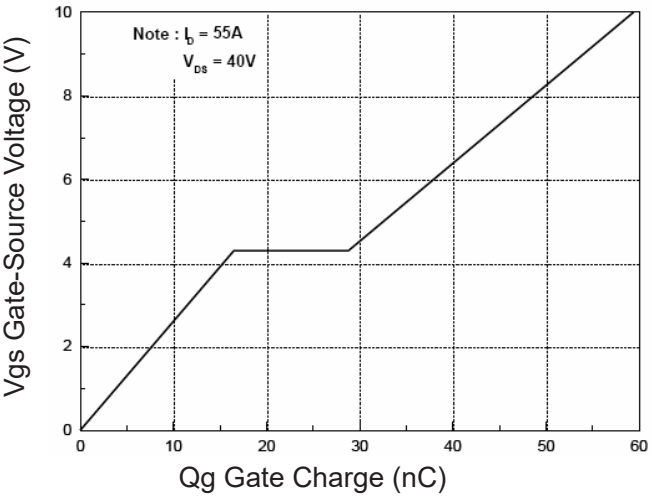



**Figure 5 Gate Charge**

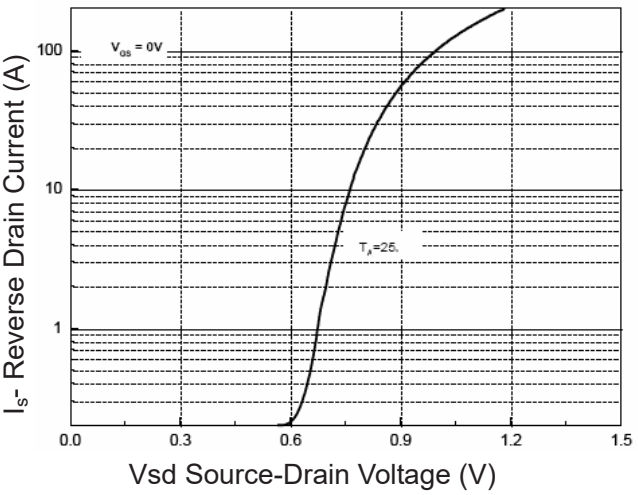



**Figure 6 Source- Drain Diode Forward**

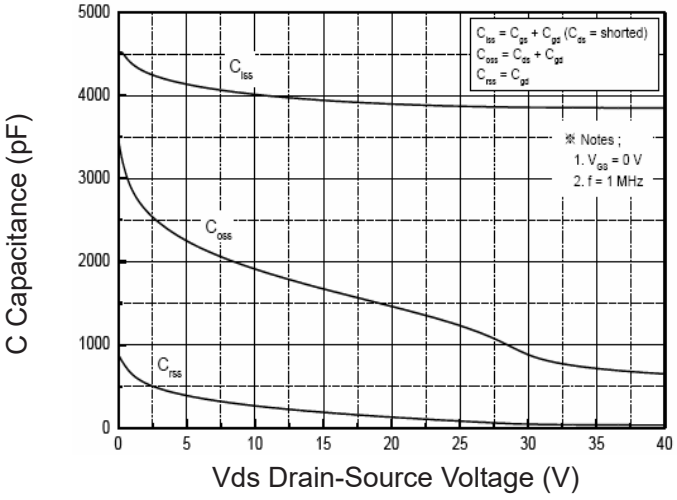



**Figure 7 Capacitance vs Vds**

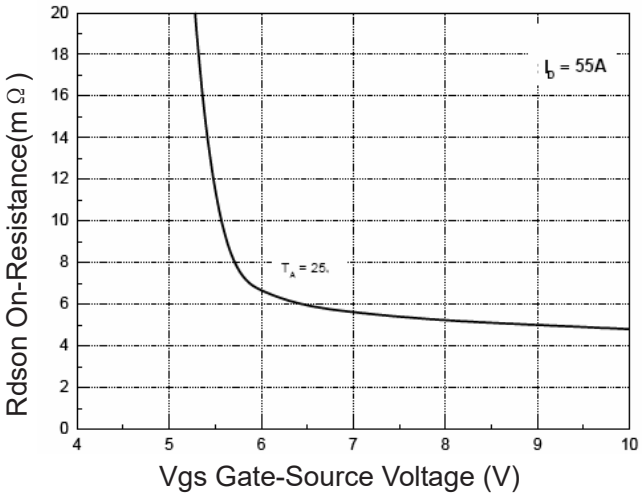



**Figure 9 Rdson vs Vgs**

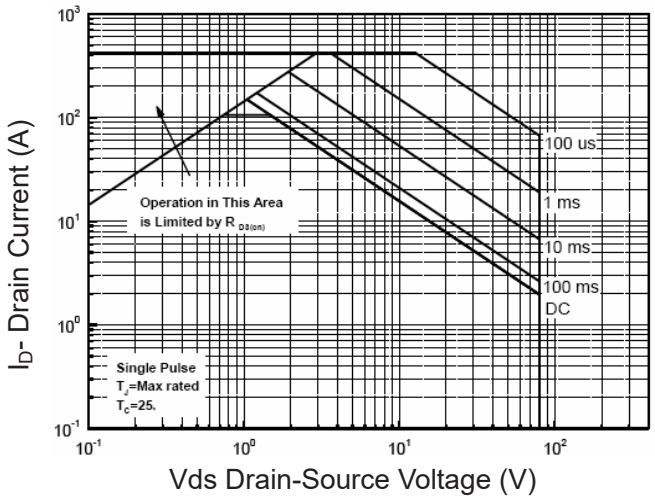



**Figure 8 Safe Operation Area**

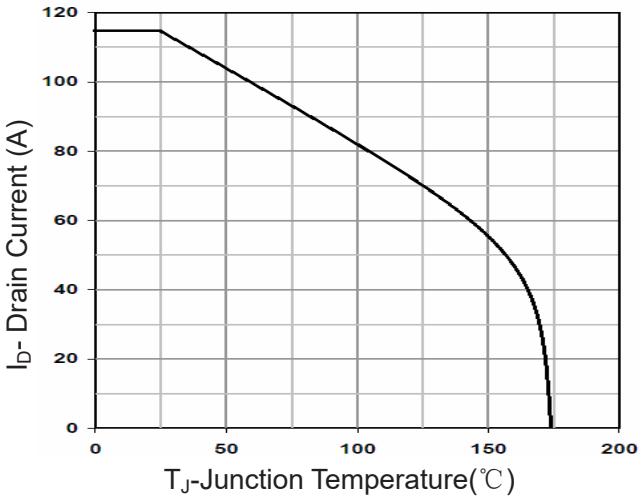



**Figure 10 Current De-rating**

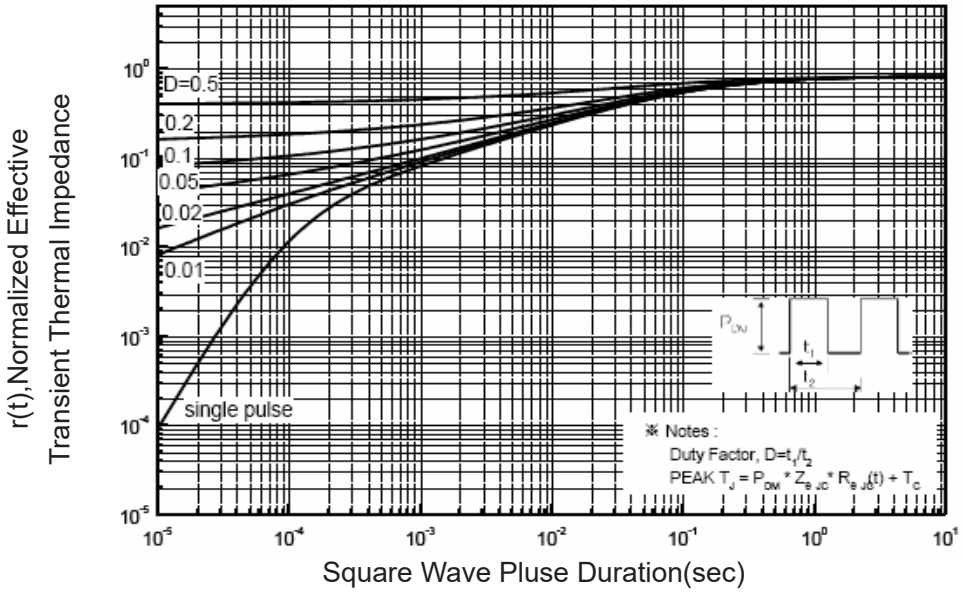



**Figure 11 Normalized Maximum Transient Thermal Impedance**