

## Description

The VST10N057 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of  $R_{DS(ON)}$  and  $Q_g$ . This device is ideal for high-frequency switching and synchronous rectification.

## General Features

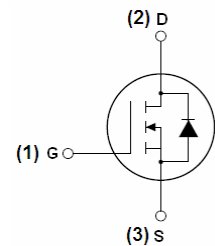
- $V_{DS} = 100V, I_D = 108A$   
 $R_{DS(ON)} = 5.7m\Omega$  (typical) @  $V_{GS} = 10V$
- Excellent gate charge x  $R_{DS(on)}$  product(FOM)
- Very low on-resistance  $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

## Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



TO-263



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST10N057-T3	VST10N057	TO-263	-	-	-

## Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous ( <b>Silicon Limited</b> )	$I_D$	108	A
Drain Current-Continuous ( <b>Package Limited</b> )	$I_D$	108	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	78	A
Pulsed Drain Current	$I_{DM}$	380	A
Maximum Power Dissipation	$P_D$	160	W
Derating factor		1.1	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	676	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

**Thermal Characteristic**

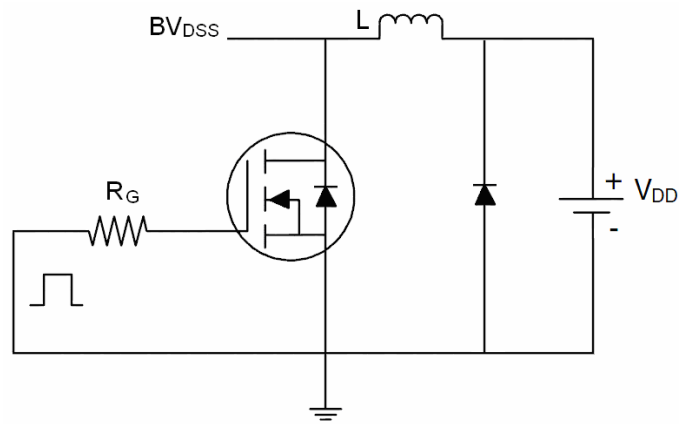
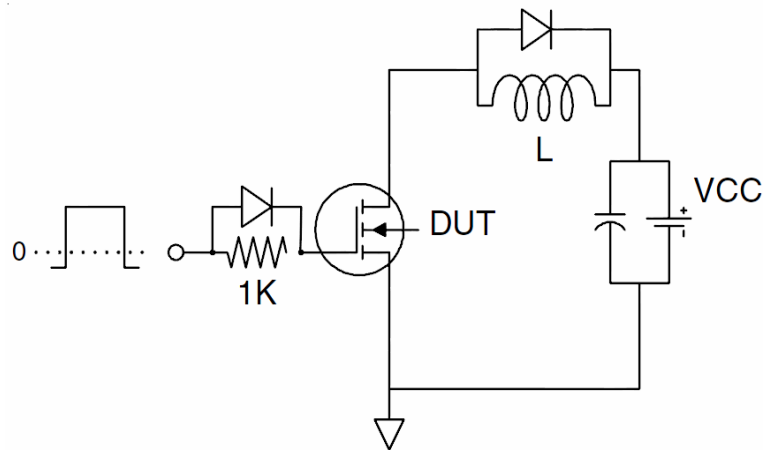
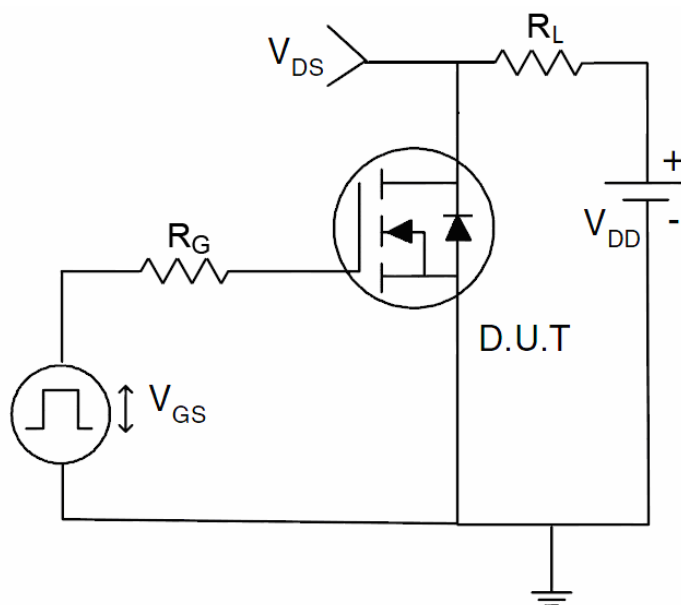
Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	0.94	$^{\circ}\text{C}/\text{W}$
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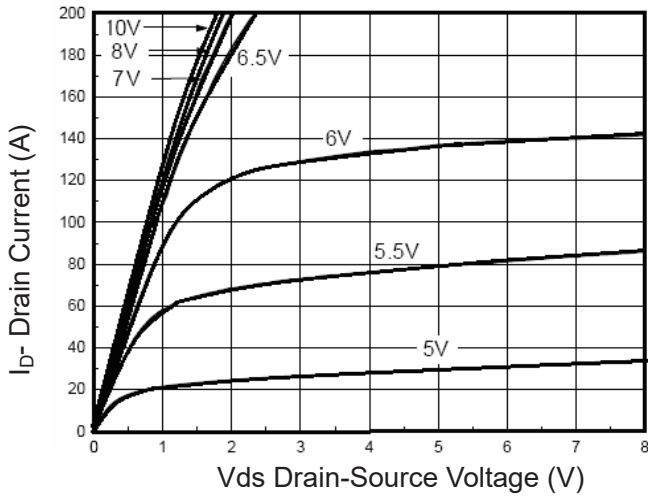
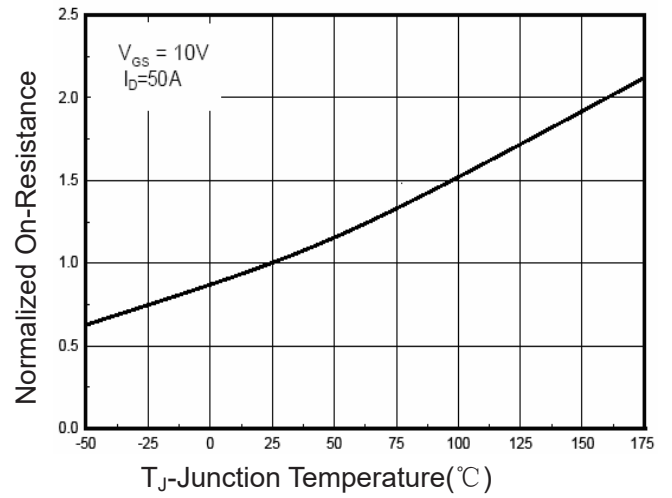
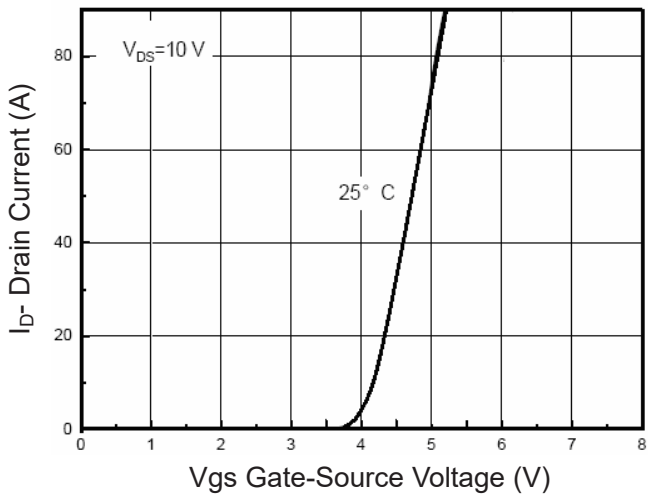
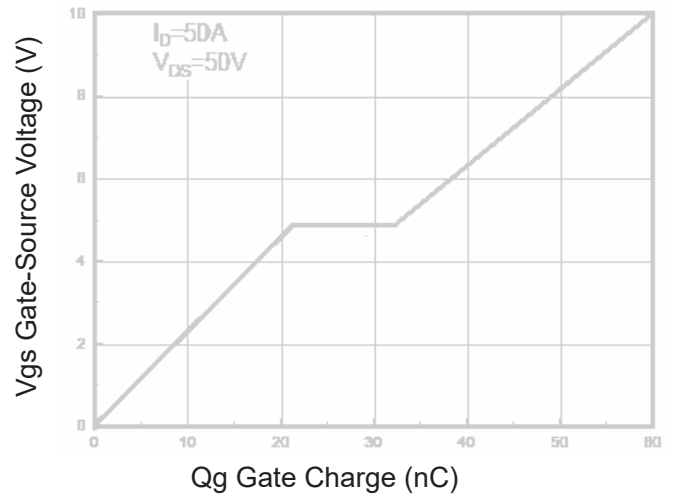
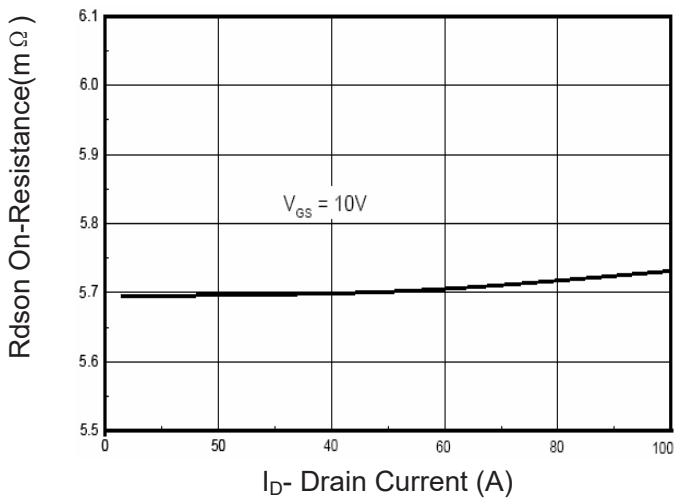
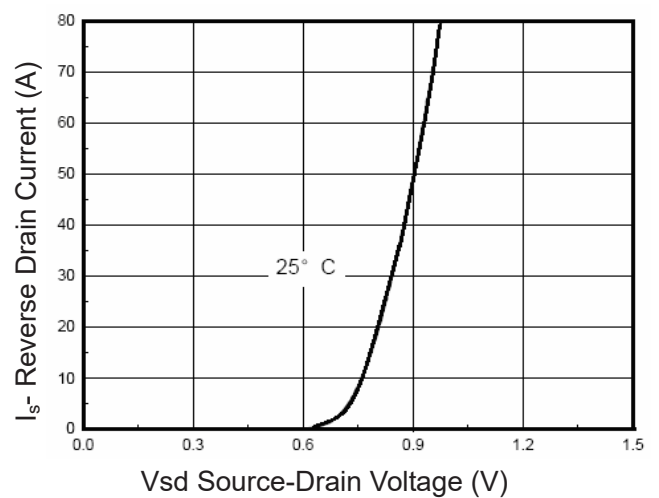
**Electrical Characteristics ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100		-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5	-	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=50A$	-	5.7	6.5	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=50A$	40	-	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	4300	-	PF
Output Capacitance	$C_{oss}$		-	790	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	47	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=50A$ $V_{GS}=10V, R_G=4.7\Omega$	-	13	-	nS
Turn-on Rise Time	$t_r$		-	58	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	39	-	nS
Turn-Off Fall Time	$t_f$		-	8	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=50V, I_D=50A,$ $V_{GS}=10V$	-	60		nC
Gate-Source Charge	$Q_{gs}$		-	21		nC
Gate-Drain Charge	$Q_{gd}$		-	11		nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=108A$	-		1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	108	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}, I_F = I_S$ $di/dt = 100A/\mu\text{s}$ <sup>(Note3)</sup>	-	60		nS
Reverse Recovery Charge	$Q_{rr}$		-	140		nC

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition :  $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

**Test Circuit**
**1)  $E_{AS}$  test Circuit**

**2) Gate charge test Circuit**

**3) Switch Time Test Circuit**


**Typical Electrical and Thermal Characteristics**

**Figure 1 Output Characteristics**

**Figure 4  $R_{dson}$ -Junction Temperature**

**Figure 2 Transfer Characteristics**

**Figure 5 Gate Charge**

**Figure 3  $R_{dson}$ - Drain Current**

**Figure 6 Source- Drain Diode Forward**

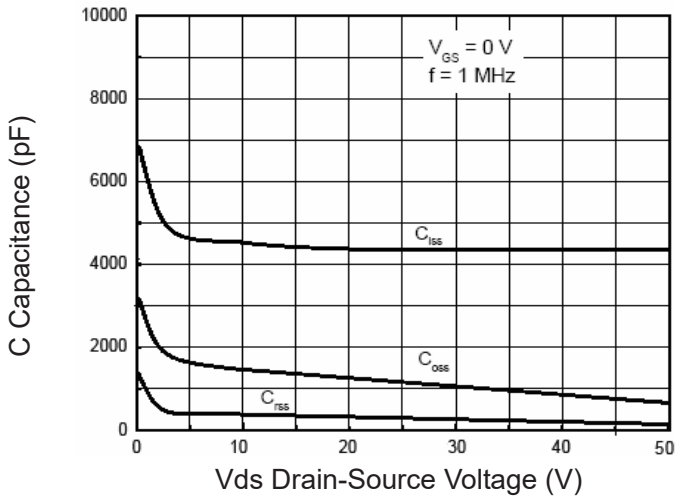


Figure 7 Capacitance vs Vds

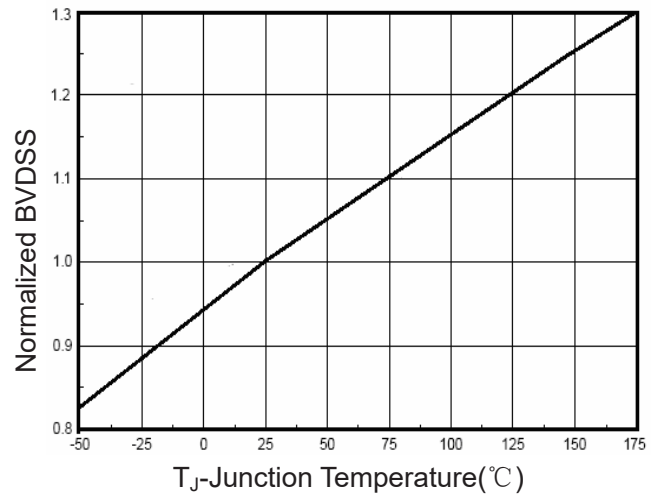


Figure 9  $BV_{DSS}$  vs Junction Temperature

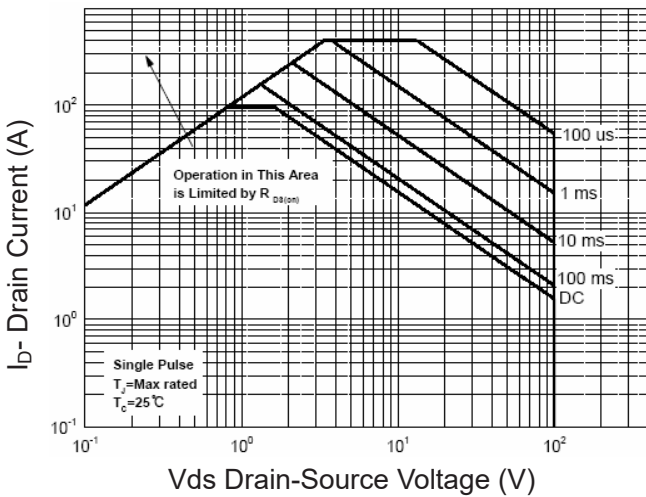


Figure 8 Safe Operation Area

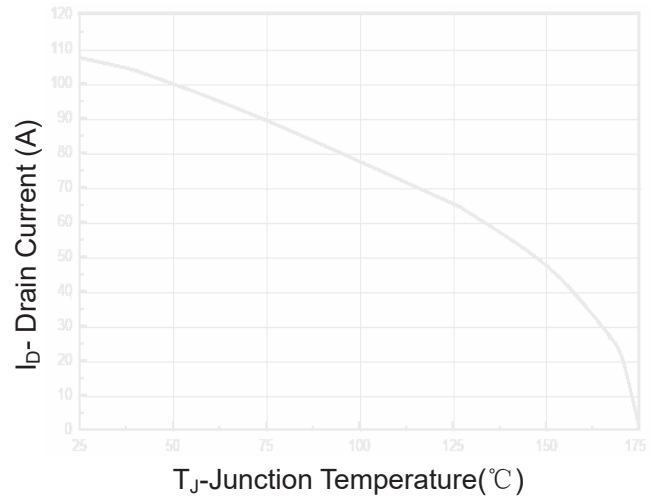


Figure 10 Current De-rating

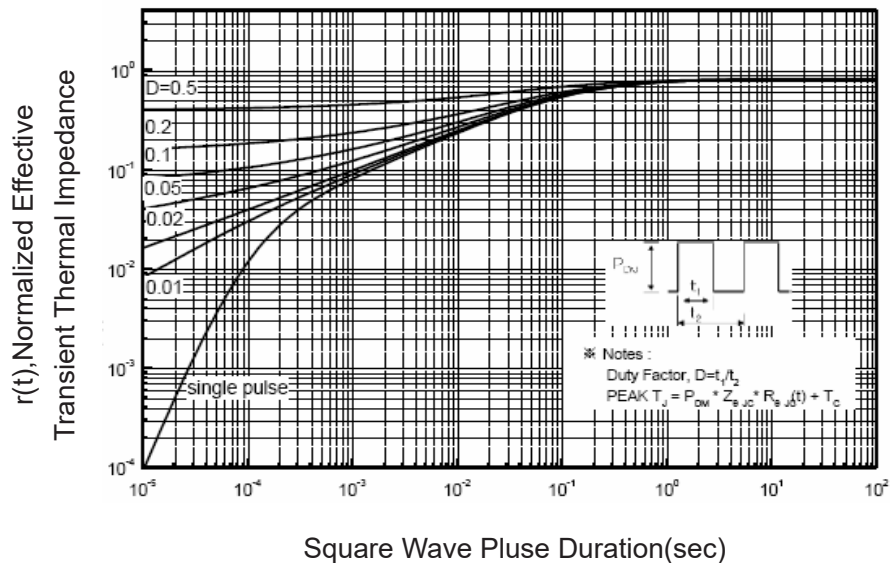


Figure 11 Normalized Maximum Transient Thermal Impedance