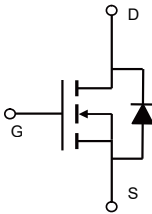## Description

These N-Channel enhancement mode power field effect transistors are using split gate trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and with stand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

◆ 100V,48A, $R_{DS(on),max}$ =8.3mΩ@V_{GS} = 10V

◆ Improved dv/dt capability

◆ Fast switching

◆ 100% EAS Guaranteed

◆ Green device available

Applications

◆ Motor Drives

◆ UPS

◆ DC-DC Converter

Product Summary

V_{DSS}	100V
$R_{DS(on),max}$@ V_{GS}=10V	8.3mΩ
I_D	48A

Pin Configuration

TO-220F

Schematic

Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	V
Continuous drain current (T_C = 25°C)	I_D	48	A
Continuous drain current (T_C = 100°C)		30	A
Pulsed drain current[1]	I_{DM}	192	A
Gate-Source voltage	V_{GSS}	±20	V
Avalanche energy[2]	E_{AS}	132	mJ
Power Dissipation (T_C = 25°C)	P_D	35	W
Storage Temperature Range	T_{STG}	-55 to +150	°C
Operating Junction Temperature Range	T_J	-55 to +150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{θJC}$	3.6	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{θJA}$	62	°C/W

Package Marking and Ordering Information

Device	Device Package	Marking	Units/Tube
VST10N071-TF	TO-220F	VST10N071-TF	50

Electrical Characteristics T_J = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0 V, I_D=250uA	100	---	---	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	2	3	4	V
Drain-source leakage current	I_{DSS}	V_{DS}=100 V, V_{GS}=0V, T_J = 25°C	---	---	1	μA
Gate leakage current, Forward	I_{GSSF}	V_{GS}=20 V, V_{DS}=0 V	---	---	100	nA
Gate leakage current, Reverse	I_{GSSR}	V_{GS}=-20 V, V_{DS}=0 V	---	---	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=30 A	---	7.4	8.3	mΩ
Forward transconductance	g_{fs}	V_{DS} =5V , I_D=30A	---	65	---	S
Dynamic characteristics						
Input capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, F = 1MHz	---	1895	---	pF
Output capacitance	C_{oss}		---	572.5	---	pF
Reverse transfer capacitance	C_{rss}		---	11.8	---	pF
Turn-on delay time	$t_{d(on)}$	V_{DD} = 50V,V_{GS}=10V, I_D = 30A	---	16.6	---	ns
Rise time	t_r		---	20	---	ns
Turn-off delay time	$t_{d(off)}$		---	68	---	ns
Fall time	t_f		---	20.8	---	ns
Gate resistance	R_g	V_{GS}=0V, V_{DS}=0V, F=1MHz	---	1.7	---	Ω
Gate charge characteristics						
Gate to source charge	Q_{gs}	V_{DS}=50 V, I_D=50A, V_{GS}= 10 V	---	10	---	nC
Gate to drain charge	Q_{gd}		---	4.2	---	nC
Gate charge total	Q_g		---	28.3	---	nC
Drain-Source diode characteristics and Maximum Ratings						
Continuous Source Current	I_S		---	---	48	A
Pulsed Source Current[3]	I_{SM}		---	---	192	A
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=30A, T_J=25℃	---	0.9	---	V
Reverse Recovery Time	t_{rr}	I_S=30A, di/dt=100A/us, T_J=25℃	---	50	---	ns
Reverse Recovery Charge	Q_{rr}		---	72	---	nC

Notes:

1: Repetitive Rating: Pulse width limited by maximum junction temperature.

2: V_{DD}=50V, V_{GS}=10V, L=0.5mH, I_{AS}=23A, R_G=25Ω, Starting T_J=25℃.
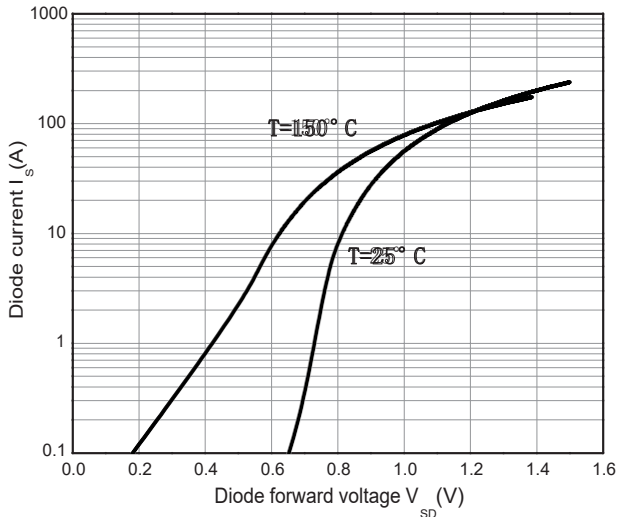
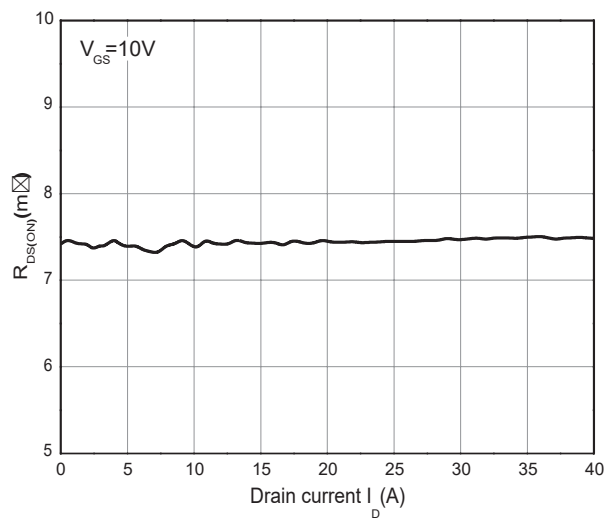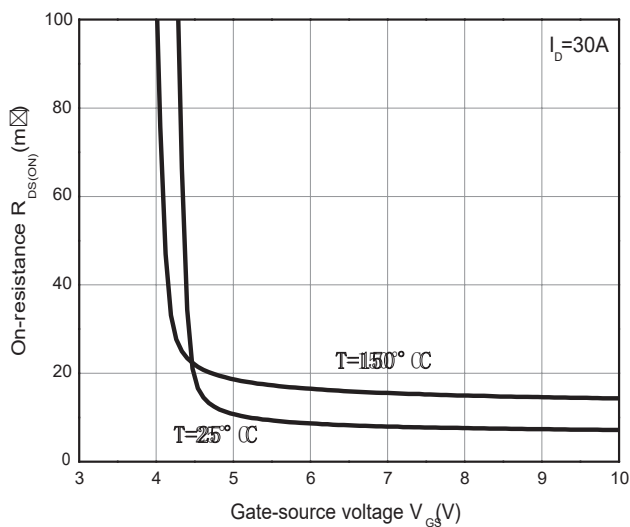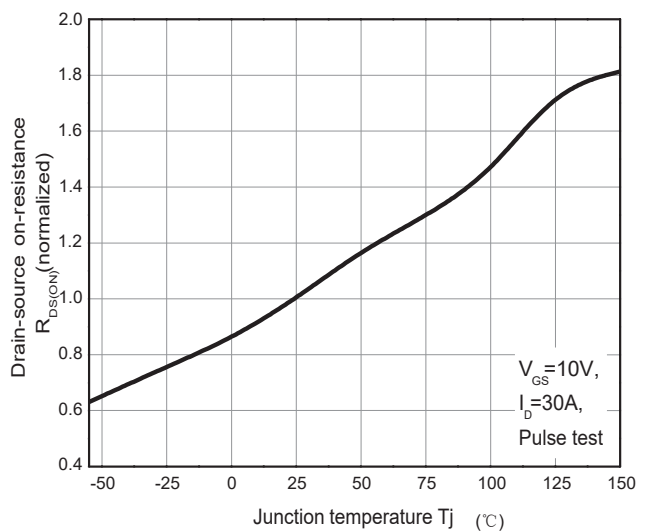3: Pulse Test：Pulse Width ≤300μs, Duty Cycle≤2％.

Electrical Characteristics Diagrams

Figure 1.On-Region Characteristics

Figure 2.Transfer Characteristics

Figure 3.Body-Diode Characteristics

Figure 4.On-Resistance Variation vs.Drain Current

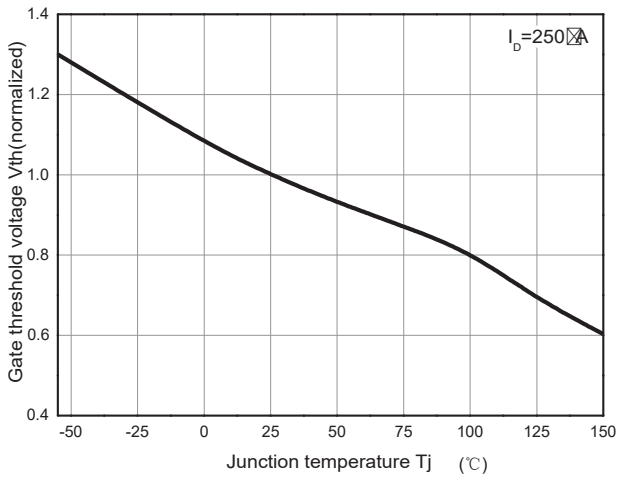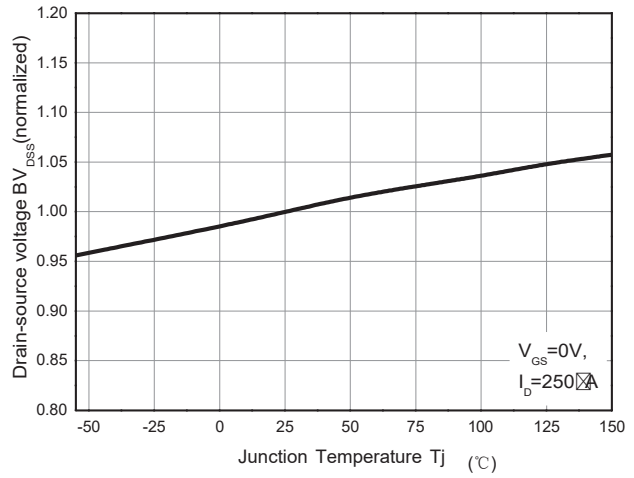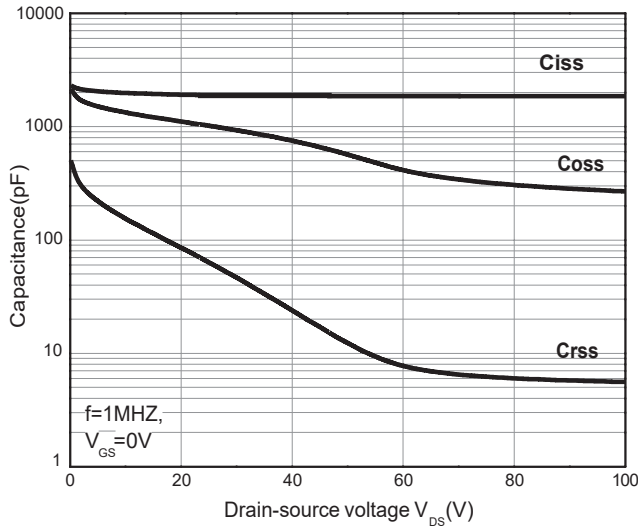Figure 5.Rds(on) vs. Gate Voltage
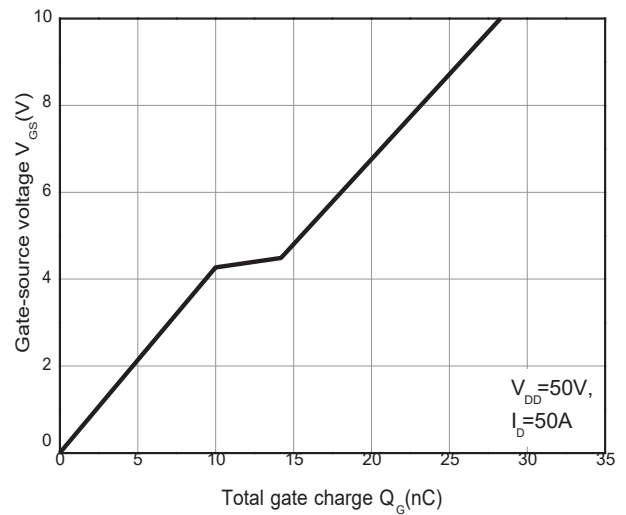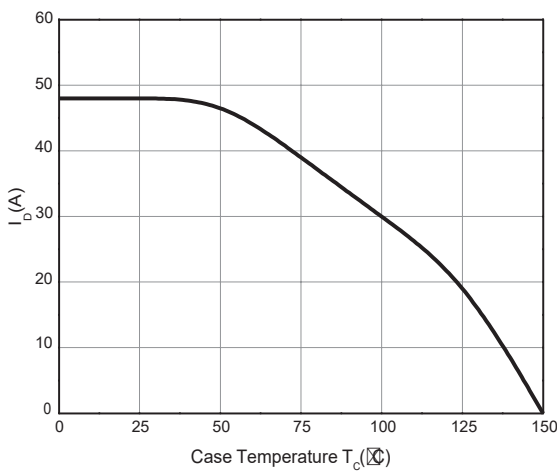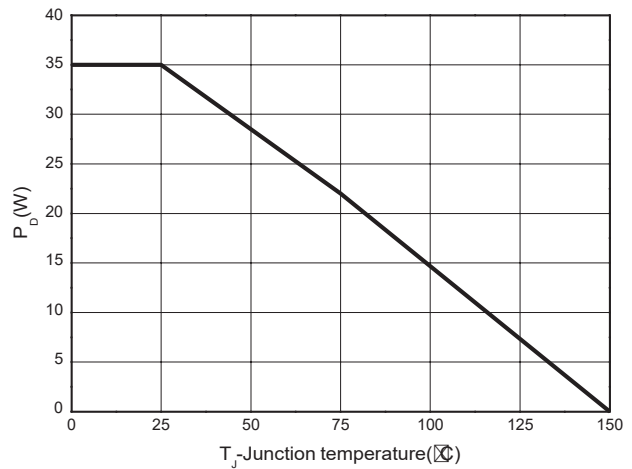

Figure 6.On-Resistance vs.Temperature

Figure 7.Threshold Voltage vs.Temperature

Figure 8.Breakdown Voltage vs.Temperature

Figure 9.Capacitance Characteristics

Figure 10.Gate Charge Characteristics

Figure 11.Drain Current Derating

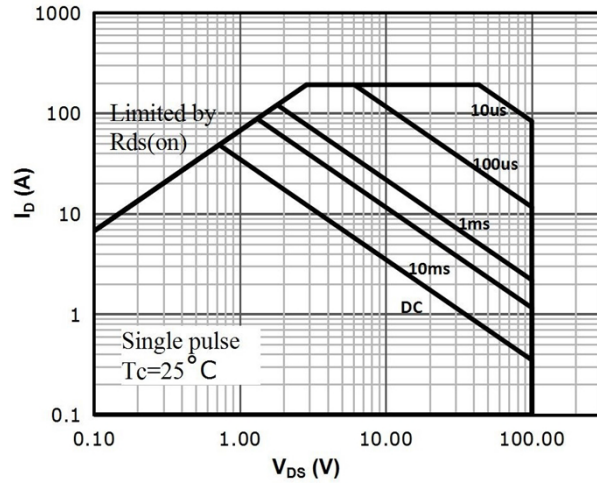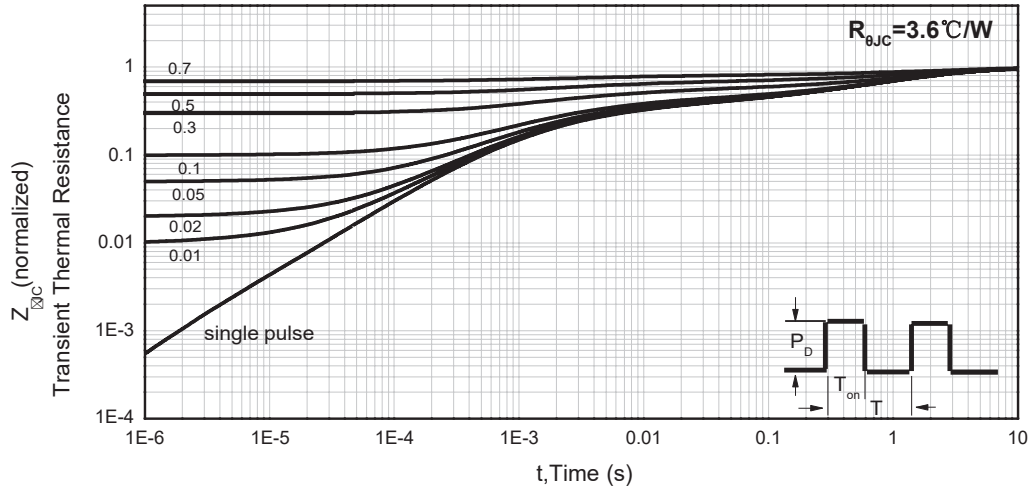Figure 12. Power Dissipation vs. Temperature

Figure 13: Safe Operating Area

Figure 14. Normalized Maximum Transient Thermal Impedance (RthJC)

Test Circuit & Waveform
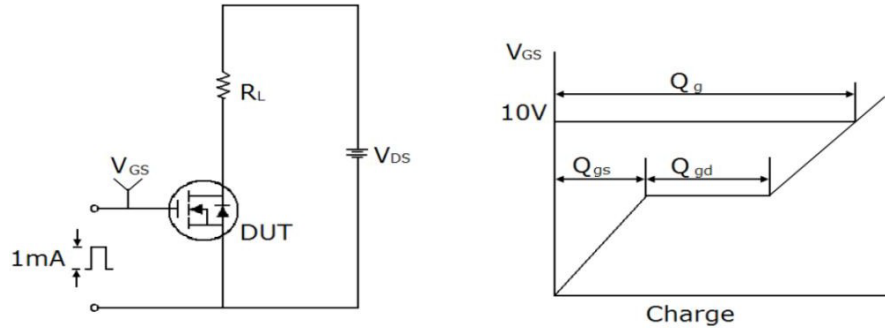
Figure 15. Gate Charge Test Circuit & Waveform

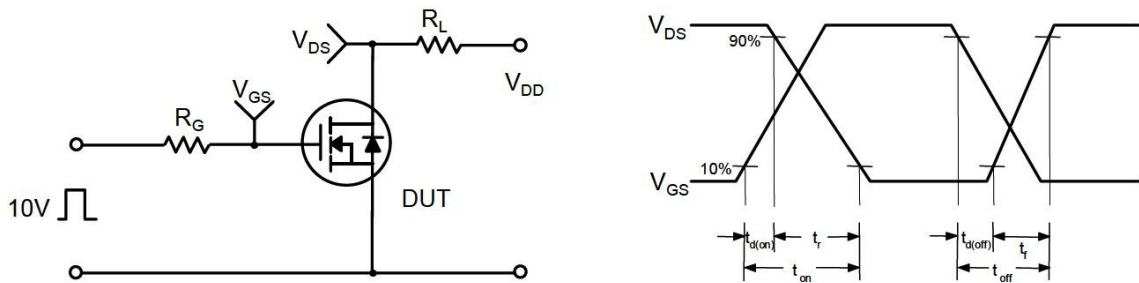Figure 16. Resistive Switching Test Circuit & Waveform

Figure 17. Unclamped Inductive Switching (UIS) Test Circuit & Waveform
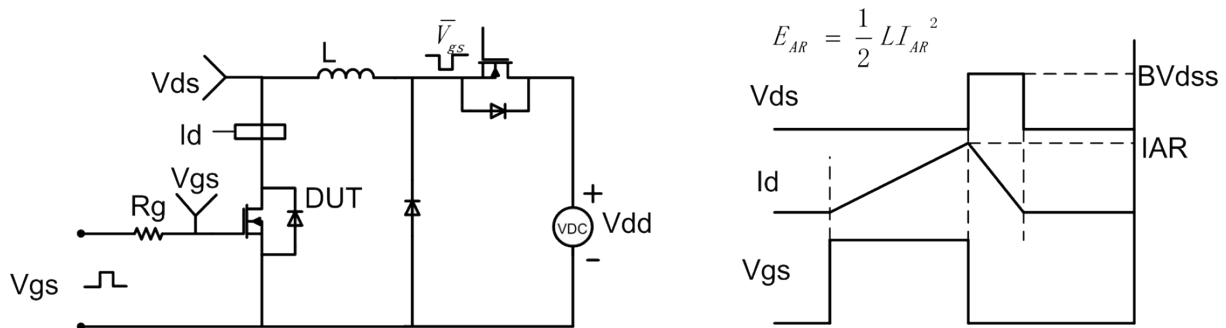
$$E_{AR} = \frac{1}{2} L I_{AR}^2$$

Figure 18. Diode Recovery Circuit & Waveform

$$Q_{rr} = -\int I dt$$