

Description

The VST13N063 uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

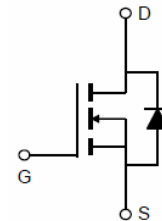
- $V_{DS} = 135V, I_D = 110A$
 $R_{DS(ON)} < 7.0m\Omega @ V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



TO-220C



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VST13N063-TC	VST13N063	TO-220C	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	135	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	110	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	93	A
Pulsed Drain Current	I_{DM}	440	A
Maximum Power Dissipation	P_D	300	W
Derating factor		2	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	1296	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

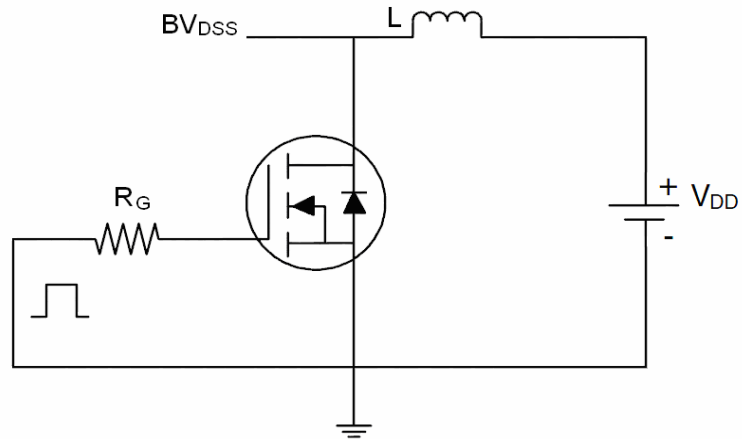
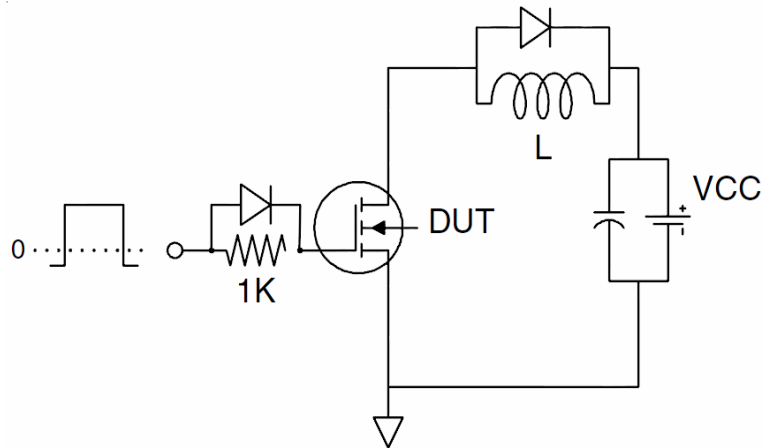
Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.5	$^{\circ}\text{C}/\text{W}$
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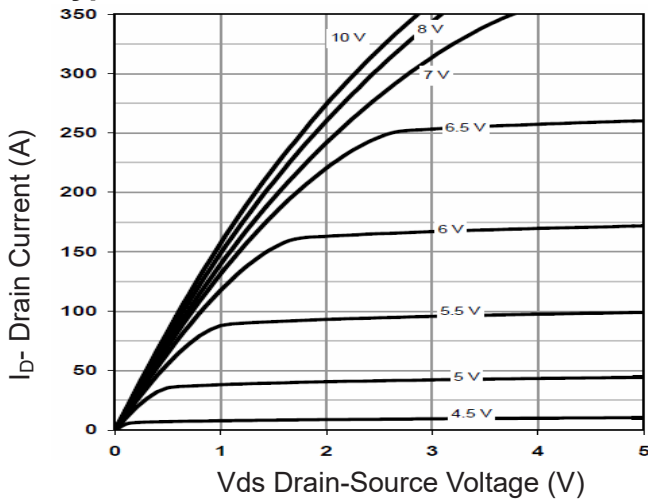
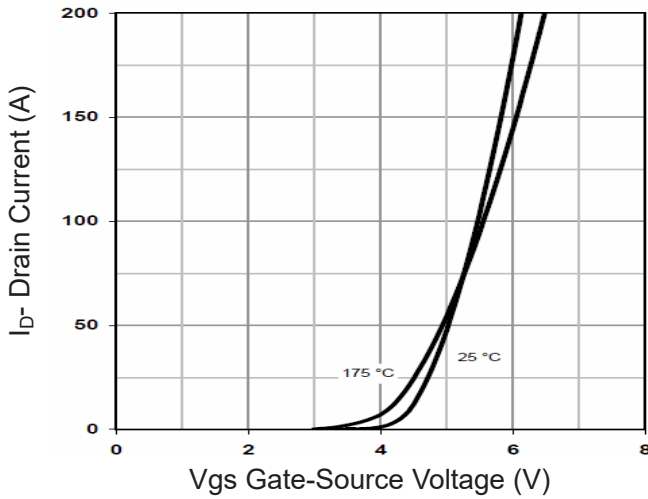
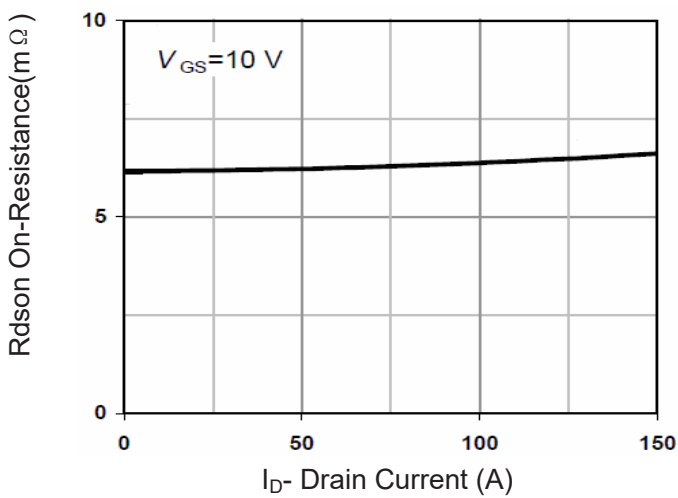
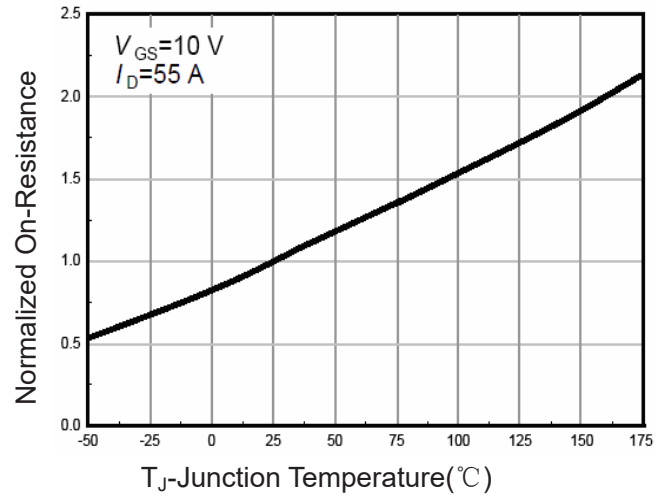
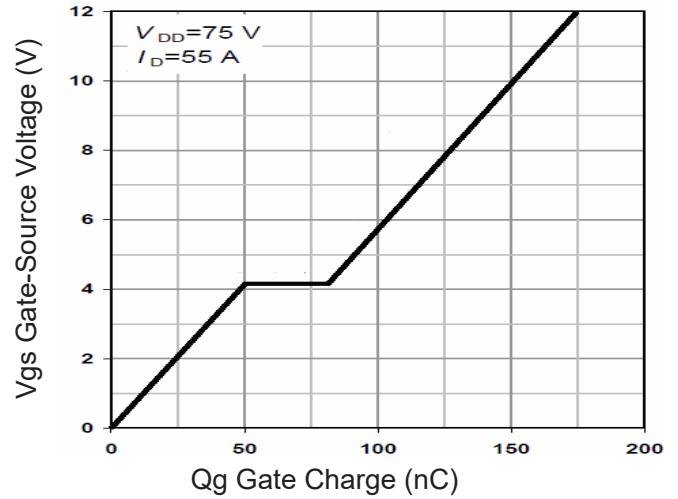
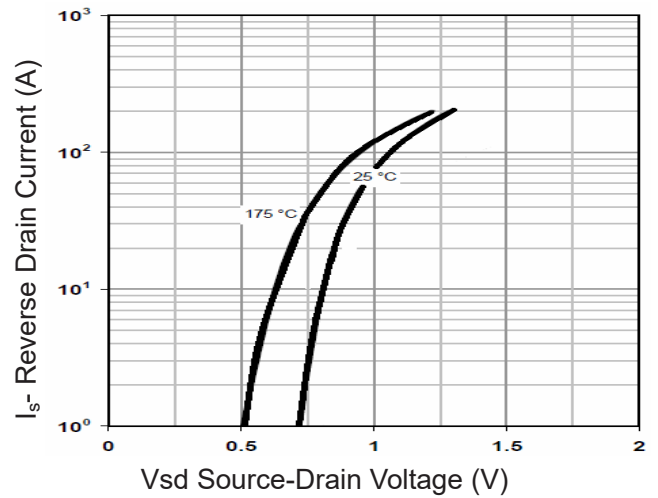
Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	135	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=135V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5	-	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=55A$	-	6.3	7.0	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=55A$	70	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=75V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	10000	-	PF
Output Capacitance	C_{oss}		-	2046	-	PF
Reverse Transfer Capacitance	C_{rss}		-	55	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=75V, I_D=55A$ $V_{GS}=10V, R_G=4.7\Omega$	-	30	-	nS
Turn-on Rise Time	t_r		-	52	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	69	-	nS
Turn-Off Fall Time	t_f		-	21	-	nS
Total Gate Charge	Q_g	$V_{DS}=75V, I_D=55A,$ $V_{GS}=10V$	-	150	-	nC
Gate-Source Charge	Q_{gs}		-	50	-	nC
Gate-Drain Charge	Q_{gd}		-	26	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_F=I_S$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	110	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}, I_F = I_S$	-	140	-	nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s$ ^(Note 3)	-	498	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Test Circuit
1) E_{AS} test Circuit

2) Gate charge test Circuit

3) Switch Time Test Circuit


Typical Electrical and Thermal Characteristics

Figure 1 Output Characteristics

Figure 2 Transfer Characteristics

Figure 3 Rdson- Drain Current

Figure 4 Rdson-Junction Temperature

Figure 5 Gate Charge

Figure 6 Source- Drain Diode Forward

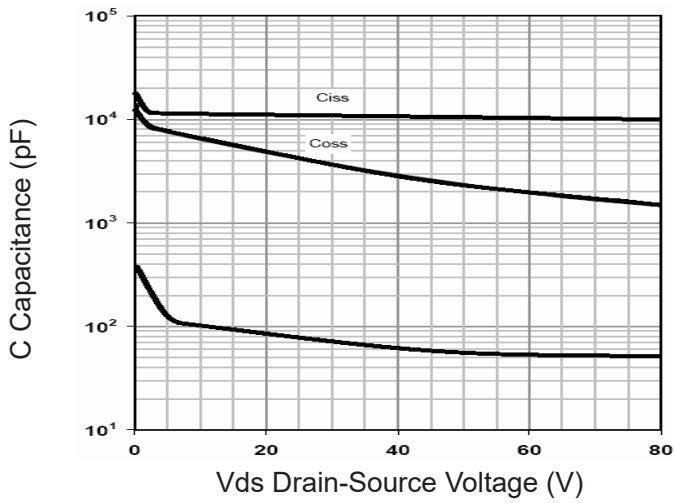


Figure 7 Capacitance vs Vds

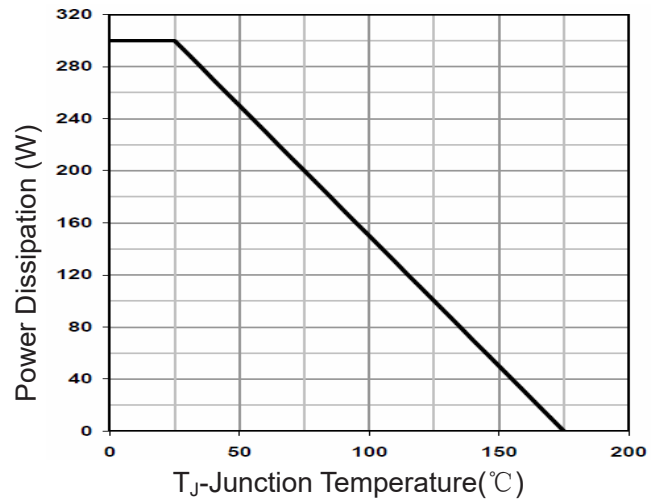


Figure 9 Power De-rating

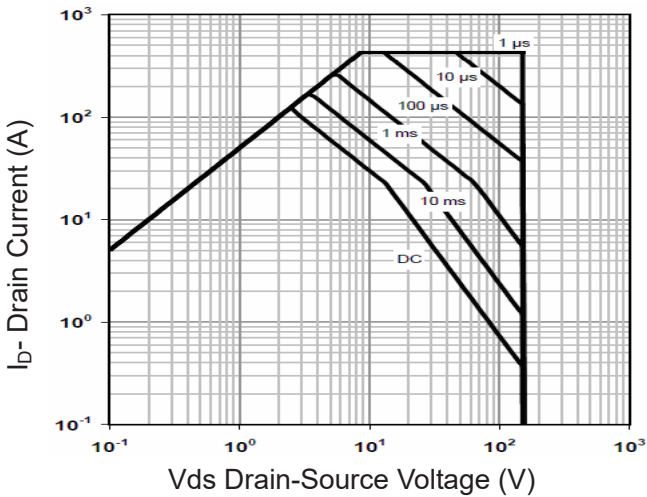


Figure 8 Safe Operation Area

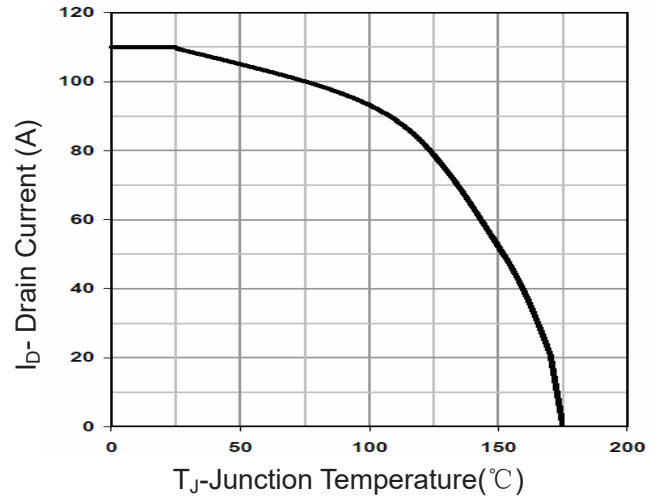


Figure 10 Current De-rating

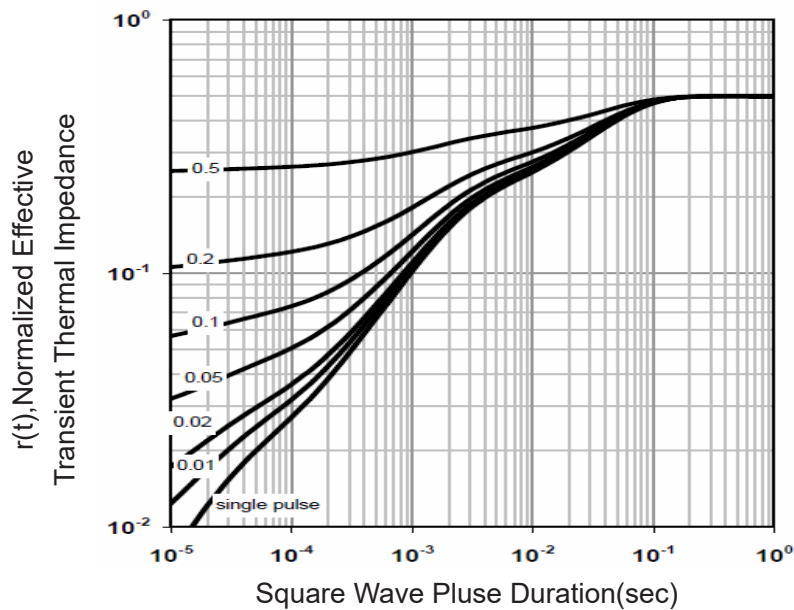


Figure 11 Normalized Maximum Transient Thermal Impedance