

Description

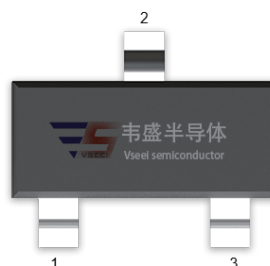
The VSM40P05Y uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

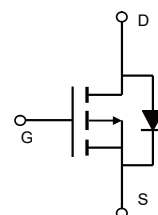
- $V_{DS} = -40V, I_D = -5.3A$
 $R_{DS(ON)} < 85m\Omega @ V_{GS} = -10V$
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- DC-DC converter



SOT-23



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM40P05Y	VSM40P05Y-S2	SOT-23	Ø180mm	8 mm	3000 units

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-5.3	A
Drain Current-Continuous($T_A = 100^\circ C$)	$I_D(100^\circ C)$	-3.7	A
Pulsed Drain Current	I_{DM}	-18	A
Maximum Power Dissipation	P_D	2	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance ,Junction-to-Case ^(Note 1)	$R_{\theta JC}$	48	$^\circ C/W$
Thermal Resistance ,Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	62.5	$^\circ C/W$

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-40V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	-1.9	-3.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-5A$	-	73	85	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-3A$	-	5	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=-20V, V_{GS}=0V,$ $F=1.0MHz$	-	600	-	pF
Output Capacitance	C_{oss}		-	90	-	pF
Reverse Transfer Capacitance	C_{rss}		-	70	-	pF
Switching Characteristics (Note 3)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-20V, R_L=2\Omega$ $V_{GS}=-10V, R_{GEN}=3\Omega$	-	9	-	nS
Turn-on Rise Time	t_r		-	8	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	28	-	nS
Turn-Off Fall Time	t_f		-	10	-	nS
Total Gate Charge	Q_g	$V_{DS}=-20V, I_D=-3A,$ $V_{GS}=-10V$	-	14	-	nC
Gate-Source Charge	Q_{gs}		-	2.9	-	nC
Gate-Drain Charge	Q_{gd}		-	3.8	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=-3.3A$	-	-	1.2	V
Diode Forward Current	I_S		-	-	-5.3	A

Notes:

1. The $R_{\theta JC}$ is the thermal impedance from junction to lead.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
3. Guaranteed by design, not subject to production.
4. These curves are based on the junction-to-ambient thermal impedance, assuming a maximum junction temperature of $T_{J(MAX)}=150^{\circ}\text{C}$. The SOA curve provides a single pulse rating.

Typical Electrical and Thermal Characteristics

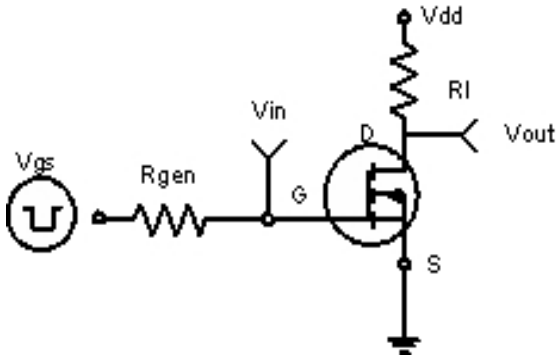


Figure 1: Switching Test Circuit

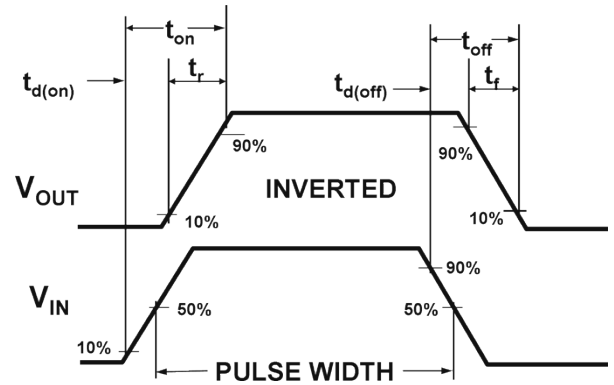


Figure 2: Switching Waveforms

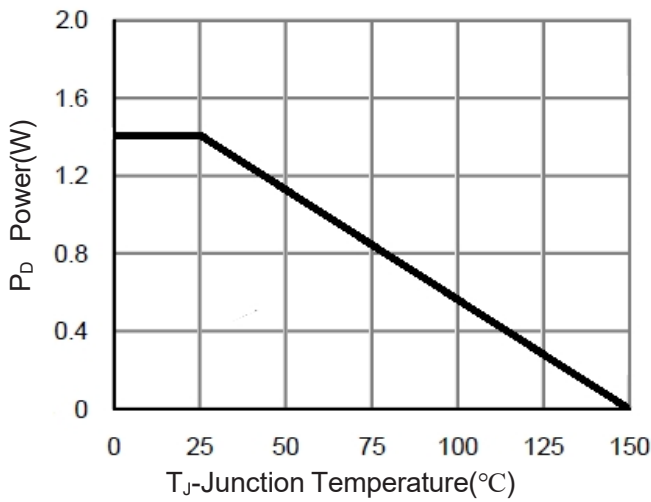


Figure 3 Power Dissipation

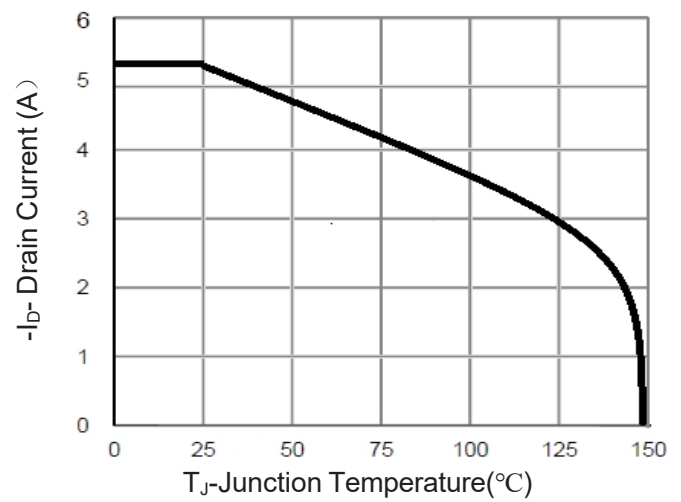


Figure 4 Drain Current

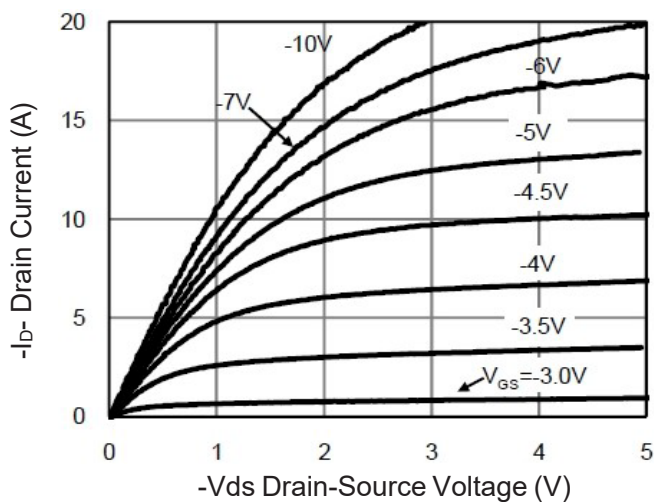


Figure 5 Output Characteristics

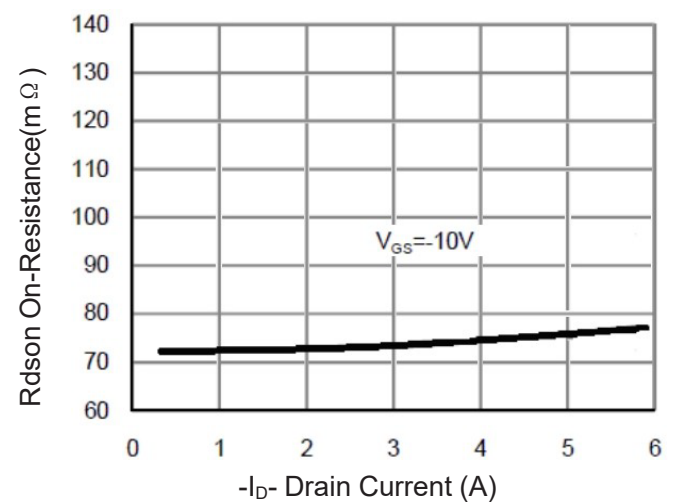
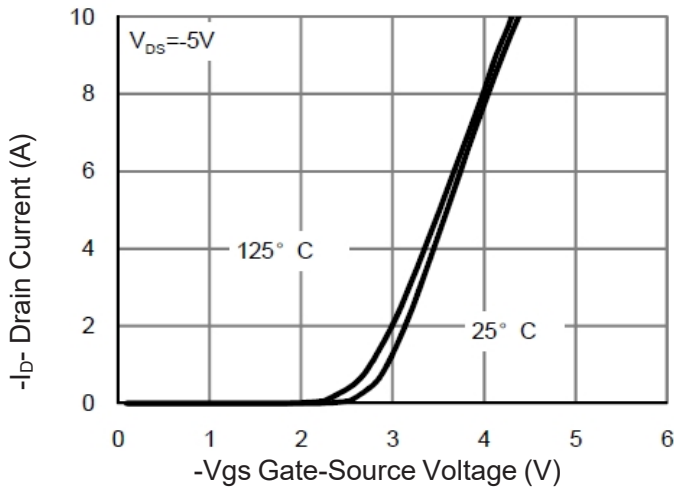
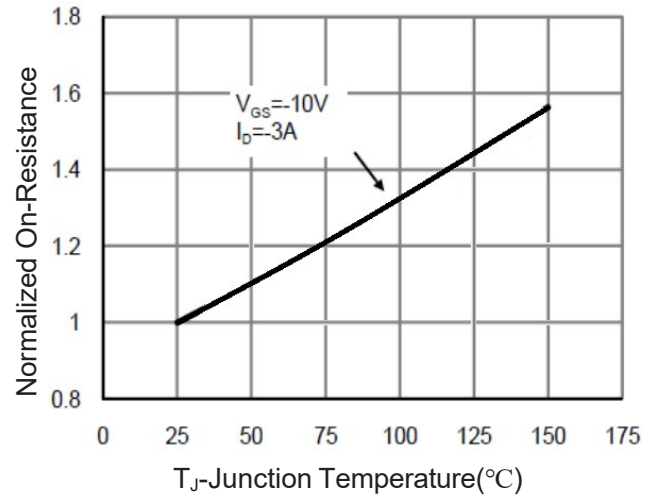
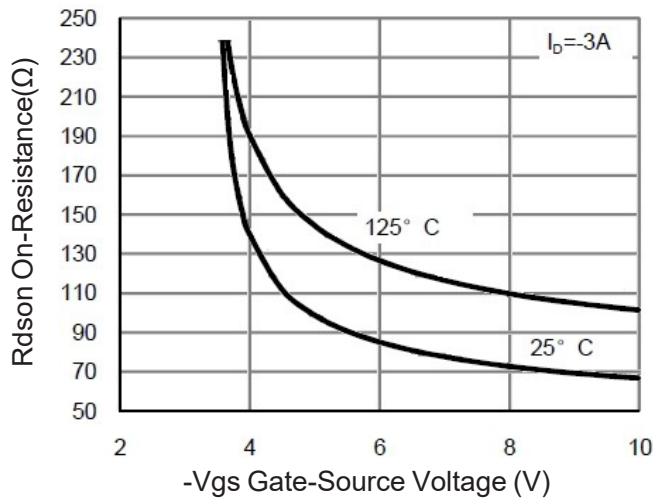
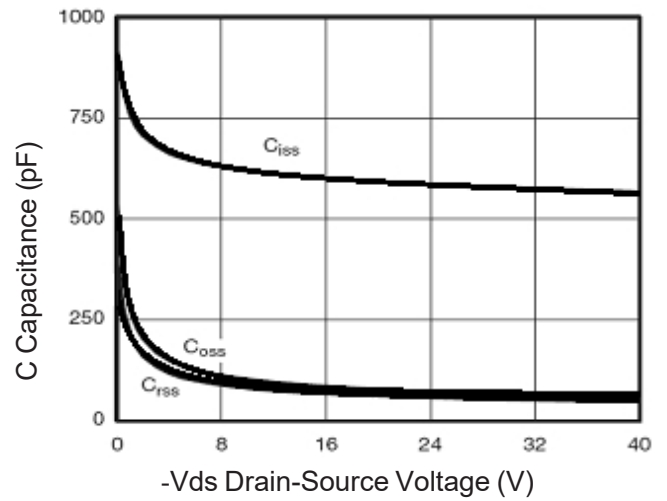
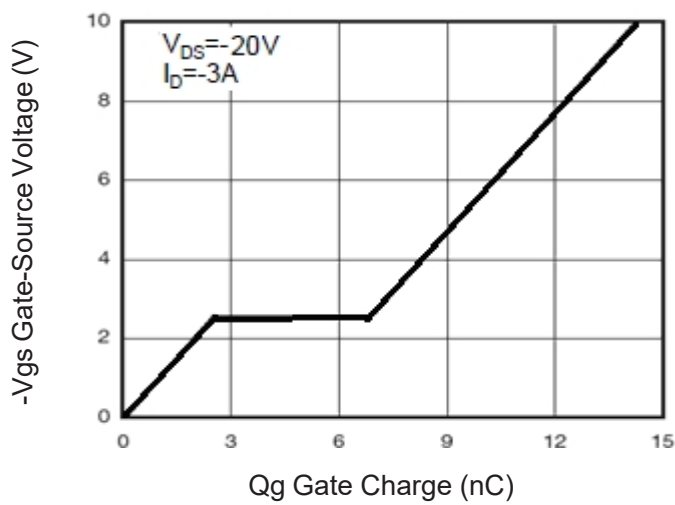
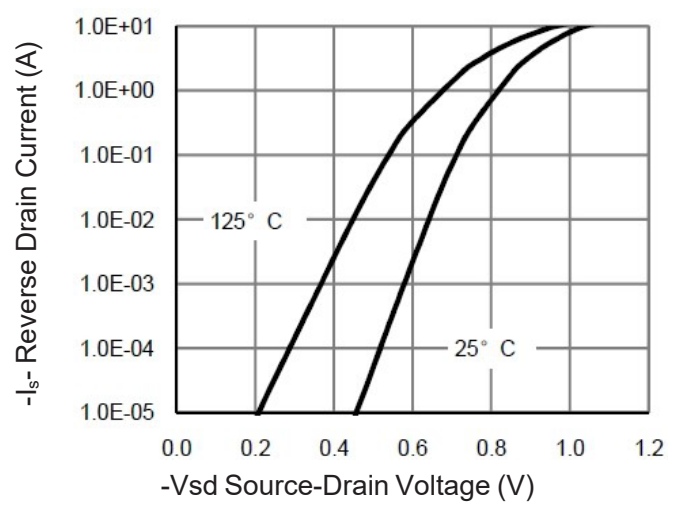


Figure 6 Drain-Source On-Resistance


Figure 7 Transfer Characteristics

Figure 8 Drain-Source On-Resistance

Figure 9 Rdson vs Vgs

Figure 10 Capacitance vs Vds

Figure 11 Gate Charge

Figure 12 Source- Drain Diode Forward

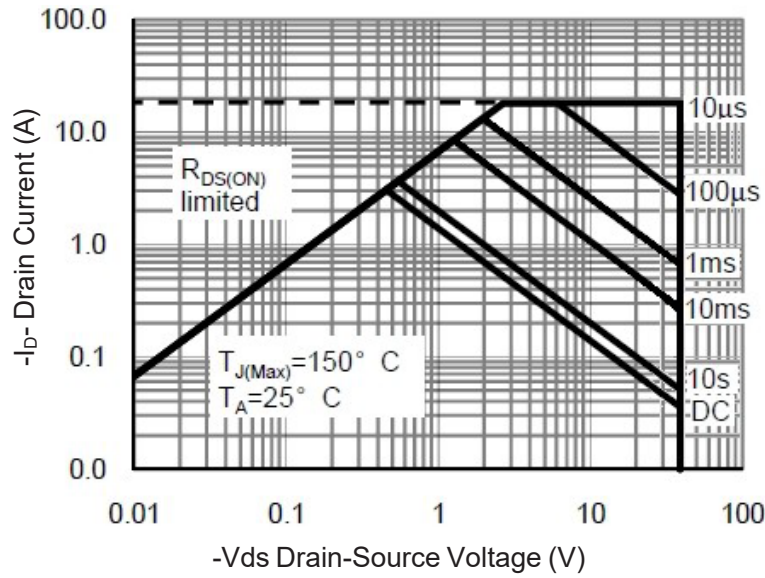


Figure 13 Safe Operation Area (Note 4)

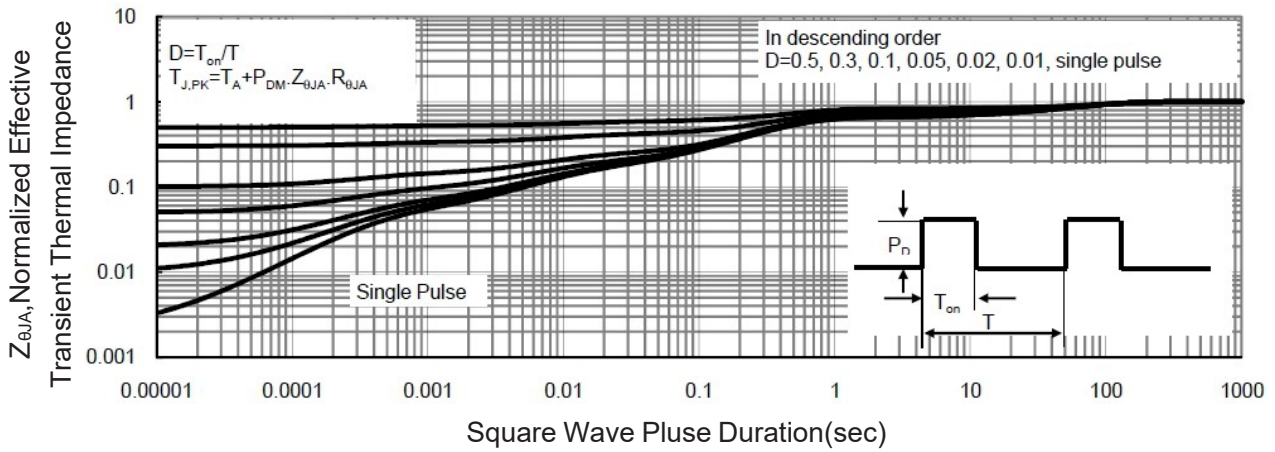


Figure 14 Normalized Maximum Transient Thermal Impedance